INA233 High-Side or Low-Side Measurement, Bidirectional Current and Power Monitor With I²C-, SMBus-, and PMBus-Compatible Interface

1 Features

- Senses Bus Voltages From 0 V to 36 V
- High-Side or Low-Side Sensing
- Reports Current, Voltage, and Power
- Integrated Power Accumulator for Energy and Average Power Monitoring
- High Accuracy:
  - 0.1% Gain Error (Max)
  - 10-µV Offset (Max)
- Configurable Averaging Options
- Independent Alert Limits for Current, Bus Voltage, and Power
- 1.8-V Compliant I²C, SMBus, PMBus Interface
- 16 Programmable Addresses
- Operates From a 2.7-V to 5.5-V Power Supply
- 10-Pin, DGS (VSSOP) Package

2 Applications

- Servers
- Telecom Infrastructure
- High-Performance Computing
- Power Metering
- Battery Chargers
- Power Supply
- Test Equipment

3 Description

The INA233 device is a current, voltage, and power monitor with an I²C-, SMBus-, and PMBus-compatible interface that is compliant with digital bus voltages from 1.8 V to 5.0 V. The device monitors and reports values for current, voltage, and power. The integrated power accumulator can be used for energy or average power calculations. Programmable calibration value, conversion times, and averaging when combined with an internal multiplier enable direct readouts of current in amperes and power in watts.

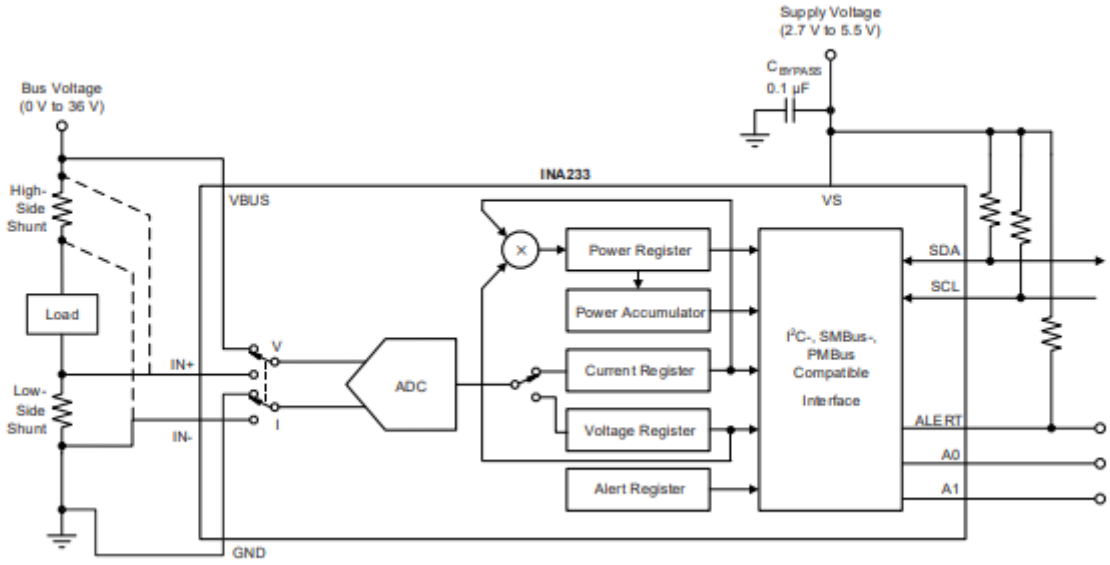
The INA233 senses current on common-mode bus voltages that can vary from 0 V to 36 V, independent of the supply voltage. The device operates from a single 2.7-V to 5.5-V supply, drawing a typical supply current of 310 µA in normal operation. The device can be placed in a low-power standby mode where the typical operating current is only 2 µA. The device is specified over the operating temperature range between –40°C and +125°C and features up to 16 programmable addresses.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA233	VSSOP (10)	3.00 mm x 3.00 mm

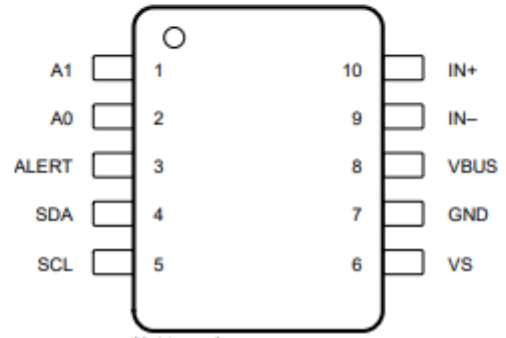
(1) For all available packages, see the orderable addendum at the end of the datasheet.

High-Side or Low-Side Sensing Application



5 Pin Configuration and Functions

DGS Package
10-Pin VSSOP
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A0	2	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 3 lists the pin settings and corresponding addresses.
A1	1	Digital input	Address pin. Connect to GND, SCL, SDA, or VS. Table 3 lists the pin settings and corresponding addresses.
ALERT	3	Digital output	PMBus-compatible multifunctional alert, open-drain output. This pin alerts on independent settings for overcurrent, under- and overvoltage, and overpower conditions.
GND	7	Analog	Ground
IN–	9	Analog input	Connect to the load side of the shunt resistor
IN+	10	Analog input	Connect to the supply side of the shunt resistor
SCL	5	Digital input	Serial bus clock line, open-drain input
SDA	4	Digital I/O	Serial bus data line, open-drain input/output
VBUS	8	Analog input	Bus voltage input
VS	6	Analog	Power supply, 2.7 V to 5.5 V

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{VS}	Supply voltage			6	V
	Analog Inputs, IN+, IN–	Differential ($V_{IN+} – V_{IN–}$)(2)	–40	40	V
		Common-mode	–0.3	40	
V_{VBUS}	VBUS pin voltage		–0.3	40	V
V_{SDA}	SDA, SCL pin voltages		GND – 0.3	6	V
V_A	A0, A1 pin voltages		GND – 0.3	6	V
I_{IN}	Input current into any pin			5	mA
I_{OUT}	Open-drain digital output current			10	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) IN+ and IN– can have a differential voltage between –40 V and 40 V. However, the voltage at these pins must not exceed the range of –0.3 V to 40 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{CM}	Common-mode input voltage	0		36	V
V_{VS}	Operating supply voltage	2.7		5.5	V
T_A	Operating free-air temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		INA233 DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	171.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	42.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	90.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

Electrical Characteristics (continued)

at T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{VBUS} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT						
	Input capacitance			3		pF
	Leakage input current	$0 V \le V_{SCL} \le V_{VS}$, $0 V \le V_{SDA} \le V_{VS}$, $0 V \le V_{Alert} \le V_{VS}$, $0 V \le V_{A0} \le V_{VS}$, $0 V \le V_{A1} \le V_{VS}$		0.5	2	µA
V_{IH}	High-level input voltage	SDA pin	1.4		6	V
V_{IL}	Low-level input voltage	SDA pin	–0.3		0.4	V
V_{OL}	Low-level output voltage	I_{OL} = 3 mA, SDA and ALERT pins	0		0.4	V
	Hysteresis			500		mV
POWER SUPPLY						
	Operating supply range		2.7		5.5	V
I_Q	Quiescent current			310	400	µA
	Quiescent current, power-down (shutdown) mode			2	5	µA
V_{POR}	Power-on-reset (POR) threshold voltage			2		V

6.5 Electrical Characteristics

at T_A = 25°C, V_{VS} = 3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{VBUS} = 12 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Shunt voltage input range		–81.92		81.9175	mV
	Bus voltage input range (1)		0		36	V
CMRR	Common-mode rejection ratio	0 V ≤ V_{IN+} ≤ 36 V	126	140		dB
V_{OS}	Offset voltage, RTI (2)	Shunt voltage		±2.5	±10	µV
		Bus voltage		±1.25	±7.5	mV
	V_{OS} (RTI (2)) vs temperature	Shunt voltage, –40°C ≤ T_A ≤ +125°C		0.02	0.1	µV/°C
		Bus voltage, –40°C ≤ T_A ≤ +125°C		10	40	
PSRR	Power-supply rejection ratio (RTI (2))	Shunt voltage, 2.7 V ≤ V_S ≤ 5.5 V		1		µV/V
		Bus voltage		0.5		mV/V
I_B	Input bias current (I_{IN+}, $I_{IN–}$ pins)			8		µA
	VBUS input impedance			830		kΩ
	Input leakage (3)	(IN+) + (IN–), power-down mode		0.1	0.5	µA
DC ACCURACY						
	ADC native resolution			16		Bits
	1-LSB step size	Shunt voltage		2.5		µV
		Bus voltage		1.25		mV
	Shunt voltage gain error			0.02%	0.1%	
	Shunt voltage gain error vs temperature	–40°C ≤ T_A ≤ +125°C		5	25	ppm/°C
	Bus voltage gain error			0.02%	0.1%	
	Bus voltage gain error vs temperature	–40°C ≤ T_A ≤ +125°C		10	50	ppm/°C
	Power gain error	V_{BUS} = 12 V, V_{IN+} – $V_{IN–}$ = –80 mV to 80 mV		0.05%	0.2%	
	Power gain error vs temperature	–40°C ≤ T_A ≤ +125°C		10	50	ppm/°C
DNL	Differential nonlinearity			±0.1		LSB
t_{CT}	ADC conversion time	CT bit = 000		140	154	µs
		CT bit = 001		204	224	
		CT bit = 010		332	365	
		CT bit = 011		588	646	
		CT bit = 100		1.1	1.21	ms
		CT bit = 101		2.116	2.328	
		CT bit = 110		4.156	4.572	
		CT bit = 111		8.244	9.068	
SMBus						
	SMBus timeout (4)			28	35	ms

(1) Although the input range is 36 V, the full-scale range of the ADC scaling is 40.96 V; see the *High-Accuracy Analog-to-Digital Convertor (ADC)* section. Do not apply more than 36 V.
(2) RTI = Referred-to-input.
(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(4) SMBus timeout in the INA233 resets the interface whenever SCL is low for more than 28 ms.