Innovative Service Around the Globe YAGEO

DATA SHEET

SURFACE-MOUNT CERAMIC MULTILAYER CAPACITORS

Ultra small: NP0/X5R/X7R/Y5V

(Pb Free & RoHS compliant)

6.3 V TO 50 V

1 pF to 100 nF

YAGEO

Product specification – Apr 19, 2006 V.2

SCOPE

This specification describes ultra small NP0/X5R/X7R/Y5V series chip capacitors with lead-free terminations.

APPLICATIONS

- Mobile phones
- Digital cameras
- Camcorders
- Tuners

FEATURES

- High capacitance per unit volume
- Supplied in bulk case or in tape on reel.

ORDERING INFORMATION

Part number is identified by the series, size, tolerance, packing style, TC material, rated voltage and capacitance value.

YAGEO ORDERING CODE

CC	XXXX	X	X	XXX	X	B	X	XXX
	(1)	(2)	(3)	(4)	(5)		(6)	(7)

(1) SIZE – INCH BASED (METRIC)

0201 (0603)

(2) TOLERANCE

C = ±0.25 pF
D = ±0.50 pF
J = ±5%
K = ±10%
M = ±20%
Z = –20/+80%

(3) PACKING STYLE

R = 7" paper tape

(4) TC MATERIAL

NPO
X5R
X7R
Y5V

(5) RATED VOLTAGE

5 = 6.3 V
6 = 10 V
7 = 16 V
8 = 25 V
9 = 50 V

(6) PROCESS

B = BME
N = NME

(7) CAPACITANCE VALUE:

First two for significant figures and 3rd for number of zero
Letter "R" for decimal point

CONSTRUCTION

The capacitor consists of a rectangular block of ceramic dielectric in which a number of interleaved metal electrodes are contained. This structure gives rise to a high capacitance per unit volume.

The inner electrodes are connected to the two end terminations and finally covered with a layer of plated tin (NiSn). The terminations are lead-free. A cross section of the structure is shown in Fig.1.

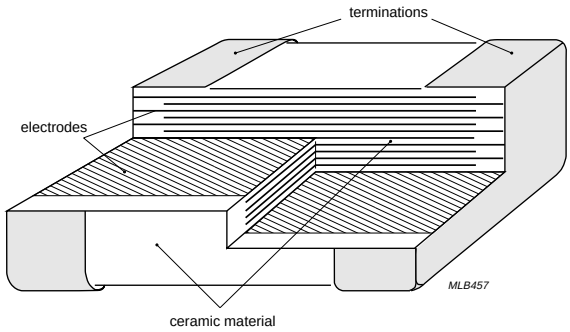

Fig. 1 Surface mounted multilayer ceramic capacitor construction

DIMENSION

For dimension see Table 1

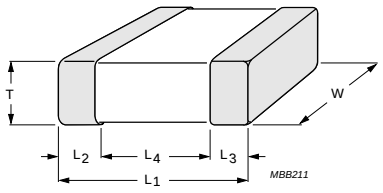

Fig. 2 Surface mounted multilayer ceramic capacitor dimension

Table 1

TYPE	L_1 (mm)	W (mm)	T (mm)	L_2/L_3 (mm)		L_4 (mm)
				min.	max.	min.
CC0201	0.6 ±0.03	0.3 ±0.03	0.3 ±0.03	0.10	0.20	0.20

CAPACITANCE RANGE & THICKNESS FOR SIZE 0201 OF NP0 25/50 V

Table 2

CAPACITANCE (pF)	0201 25 V	0201 50 V
1.0		0.3 ±0.03
1.2		
1.5		
1.8		
2.2		
2.7		
3.3		
3.9		
4.7		
5.6		
6.8		
8.2		
10		
12		
15		
18		
22		
27	0.3 ±0.03	
33		
39		
47		
56		
68		
82		
100		

NOTE

1. Values in shaded cells indicate thickness class in mm.
2. Capacitance range < 1 pF is on request.

CAPACITANCE RANGE & THICKNESS FOR SIZE 0201 OF X5R/X7R/Y5V/ 6.3/10/16/25/50 V

Table 3

CAPACITANCE	X5R	X7R				Y5V
(nF)	6.3 V	10 V	16 V	25 V	50 V	6.3 V
0.047					0.3 ±0.03	
0.068						
0.10						
0.15						
0.22						
0.33						
0.47						
0.68				0.3 ±0.03		
1.0		0.3 ±0.03	0.3 ±0.03			
1.5						
2.2						
3.3						
4.7						
6.8						
10						
15						
22						
33						
47						
68						
100	0.3 ±0.03					0.3 ±0.03

NOTE

1. Values in shaded cells indicate thickness class in mm.

THICKNESS CLASSES AND PACKING QUANTITY

Table 4

DESCRIPTION	SIZE CODE	THICKNESS CLASSIFICATION (mm)	8 mm TAPE WIDTH/AMOUNT PER REEL				12 mm TAPE WIDTH /AMOUNT PER REEL	AMOUNT PER BULK CASE
			Ø180 mm, 7"		Ø330 mm, 13"			
			Paper	Blister	Paper	Blister	Ø180 mm, 7" Blister	
Discrete capacitors	0201	0.3 ±0.03	15,000	---	50,000	---	---	---
	0402	0.5 ±0.05	10,000	---	50,000	---	---	50,000
	0603	0.8 ±0.07	4,000	---	15,000	---	---	15,000
	0805	0.6 ±0.10	4,000	---	20,000	---	---	10,000
		0.85 ±0.1	4,000	---	15,000	---	---	8,000
		1.25 ±0.10	---	3,000	---	10,000	---	5,000
	1206	0.6 ±0.10	4,000	---	20,000	---	---	---
		0.85 ±0.10	4,000	---	15,000	---	---	---
		1.00 / 1.15 ±0.10	---	3,000	---	10,000	---	---
		1.6 ±0.15	---	2 500	---	10,000	---	---
		1.6 ±0.20	---	2,000	---	10,000	---	---
	1210	0.6 / 0.7 ±0.10	---	4,000	---	15,000	---	---
		0.85 ±0.10	---	4,000	---	10,000	---	---
		1.15 ±0.10	---	3,000	---	10,000	---	---
		1.15 ±0.15	---	3,000	---	10,000	---	---
		1.5 ±0.10	---	2,000	---	---	---	---
		1.6 / 1.9 ±0.20	---	2,000	---	---	---	---
		2.5 ±0.20	---	1,000	---	---	---	---
	1808	1.15 ±0.15	---	---	---	---	1 500	---
		1.35 ±0.15	---	---	---	---	1,000	---
		1.5 ±0.10	---	---	---	---	1,000	---
	1812	0.6 / 0.85 ±0.10	---	---	---	---	2,000	---
		1.15 ±0.10	---	---	---	---	1,500	---
		1.15 ±0.15	---	---	---	---	1,500	---
		1.35 ±0.15	---	---	---	---	1,000	---
		1.5 ±0.1	---	---	---	---	1,000	---
		1.6 ±0.2	---	---	---	---	1,000	---
Arrays	0508	0.6 ±0.10	4,000	---	---	---	---	---
		0.85 ±0.10	4,000	---	---	---	---	---
	0612	0.8 ±0.10	4,000	---	---	---	---	---
		1.2 ±0.10	---	3,000	---	---	---	---

NOTE

1. For bulk case, tape and reel specification/dimensions, please see the special data sheet "Packing" document.

ELECTRICAL CHARACTERISTICS

NP0/X5R/X7R/Y5V DIELECTRIC CAPACITORS; NISN TERMINATIONS

Unless otherwise stated all electrical values apply at an ambient temperature of 20±1 °C, an atmospheric pressure of 86 to 106 kPa, and a relative humidity of 63 to 67%.

Table 5

DESCRIPTION	VALUE
Capacitance range (1) :	
NP0	1 pF to 100 pF
X5R/Y5V	100 nF
X7R	47 pF to 10 nF
RATED VOLTAGE U_r (DC):	
NP0	25/50 V
X5R/Y5V	6.3 V
X7R	10/16/25/50 V
Capacitance tolerance (1):	
NP0	C <10 pF: ±0.25 pF, ±0.50 pF; C ≥10 pF: ±5%
X5R	±10%
X7R	±10%
Y5V	–20% ~ +80%
Dissipation factor (D.F.) (1) (max.):	
NP0	C ≤10 pF: $D.F.=\frac{30+7C}{100\times C}$ or 0.3%; whichever is smallest; C >10 pF: 0.1%
X5R	10%
X7R	10 V: 5%; 16 V: 3.5%; 25/50 V: 2.5%
Y5V	15%
Insulation resistance after 1 minute at Ur (DC)	R_{ins} ≥ 10 GΩ or R_{ins} × C ≥ 500 seconds whichever is less
Maximum capacitance change as a function of temperature (temperature characteristic/coefficient):	
NP0	±30 ppm/°C
X5R/X7R	±15%
Y5V	+22% ~ –82%
Operating temperature range:	
NP0/X7R	–55 °C to +125 °C
X5R	–55 °C to +85 °C
Y5V	–30 °C to +85 °C

NOTE

1. f=1 KHz for C ≤ 10 μF; measuring at voltage 1 V_{rms}; f=120 Hz for C > 10 μF; measuring at voltage 0.5 V_{rms}.

TESTS AND REQUIREMENTS

Table 6 Test condition, procedure and requirements

TEST	TEST METHOD		PROCEDURE	REQUIREMENTS
Mounting	IEC 60384-21/22	4.3	The capacitors may be mounted on printed-circuit boards or ceramic substrates	No visible damage
Visual inspection and dimension check		4.4	Any applicable method using × 10 magnification	In accordance with specification
Capacitance		4.5.1	NP0: f = 1 MHz for C ≤ 1 nF, measuring at voltage 1 V_{rms} at 20 °C; f = 1 KHz for C > 1 nF, measuring at voltage 1 V_{rms} at 20 °C X5R/X7R/Y5V: f = 1 KHz for C ≤ 10 μF, measuring at voltage 1 V_{rms} at 20 °C	Within specified tolerance
Dissipation factor (D.F.)		4.5.2	NP0: f = 1 MHz for C ≤ 1 nF, measuring at voltage 1 V_{rms} at 20 °C; f = 1 KHz for C > 1 nF, measuring at voltage 1 V_{rms} at 20 °C X5R/X7R/Y5V: f = 1 KHz for C ≤ 10 μF, measuring at voltage 1 V_{rms} at 20 °C	In accordance with specification
Insulation resistance		4.5.3	At U_r (DC) for 1 minute	In accordance with specification
Voltage proof		4.5.4.2	Test voltage (DC) applied for 1 minute U_r ≤ 100 V: 2.5 × U_r applied to NP0/X5R/X7R/Y5V series 100 V < U_r ≤ 200 V: 1.5 × U_r + 100 V applied to NP0/X7R series 200 V < U_r ≤ 500 V: 1.3 × U_r + 100 V applied to NP0/X7R series U_r > 500 V: 1.3 × U_r applied to NP0/X7R series I: 7.5 mA	No breakdown or flashover
Temperature characteristic		4.6	Between minimum and maximum temperature	NP0: ΔC/C: ±30 ppm/°C X5R/X7R: ΔC/C: ±15% Y5V: ΔC/C: +22%~ –82%
Adhesion		4.15	A force applied for 10 seconds to the line joining the terminations and in a plane parallel to the substrate for size ≥ 0603: a force of 5 N applied for size 0402: a force of 2.5 N applied for size 0201: a force of 1 N applied	No visible damage

Table 6 Test condition, procedure and requirements (continued)

TEST	TEST METHOD		PROCEDURE	REQUIREMENTS
Bond strength of plating on end face	IEC 60384-21/22	4.8	Mounting in accordance with IEC 60384-22 paragraph 4.3 Conditions: bending 1 mm at a rate of 1 mm/s, radius jig 340 mm	No visible damage NP0: $\lvert\Delta C/C\rvert$: ≤ 1% or 0.5 pF whichever is greater X5R/X7R/Y5V: $\lvert\Delta C/C\rvert$: ≤ 10%
Resistance to soldering heat		4.9	Precondition: 150 +0/–10 °C for 1 hour, then keep for 24 ±1 hours at room temperature Preheating: for size ≤ 1206: 120 to 150 °C for 1 minute Preheating: for size >1206: 100 to 120 °C for 1 minute and 170 to 200 °C for 1 minute Solder bath temperature: 260 ±5 °C Dipping time: 10 ±0.5 seconds Recovery time: 24 ±2 hours.	The termination shall be well tinned NP0: $\lvert\Delta C/C\rvert$: ≤ 0.5% or 0.5 pF whichever is greater X5R/X7R: $\lvert\Delta C/C\rvert$: ≤ 10% Y5V: $\lvert\Delta C/C\rvert$: ≤ 20% D.F.: within initial specified value R_{ins}: within initial specified value
Solderability		4.10	Unmounted chips completely immersed in a solder bath at 235 ±5 °C Dipping time: 2 ±0.5 seconds Depth of immersion: 10 mm	The termination shall be well tinned.
Rapid change of temperature		4.11	Preconditioning; 150 +0/–10 °C for 1 hour, then keep for 24 ±1 hours at room temperature 5 cycles with following detail: 30 minutes at lower category temperature; 30 minutes at upper category temperature Recovery time 24 ±2 hours.	No visual damage NP0: $\lvert\Delta C/C\rvert$: ≤ 1% or 1 pF whichever is greater X5R/X7R: $\lvert\Delta C/C\rvert$: ≤ 15% Y5V: $\lvert\Delta C/C\rvert$: ≤ 20% D.F.: within initial specified value R_{ins}: within initial specified value
Damp heat, with U_r load		4.13	Initial measurements; after 150 +0/-10 °C for 1 hour, then keep for 24 ±1 hours at room temperature Duration and conditions: 500 ±12 hours at 40 ±2 °C; 90 to 95% RH; U_r applied Final measurement: perform a heat treatment at 150 +0/–10 °C for 1 hour, final measurements shall be carried out 24 ±1 hours after recovery at room temperature without load.	NP0: $\lvert\Delta C/C\rvert$: ≤ 2% or 1 pF whichever is greater X5R/X7R: $\lvert\Delta C/C\rvert$: ≤ 20% Y5V: $\lvert\Delta C/C\rvert$: ≤ 30% NP0/X5R/X7R/Y5V: D.F.: 2 × initial value max. NP0: R_{ins} ≥ 2,500 MΩ or $R_{ins} \times C_r$ ≥ 25 seconds, whichever is less X5R/X7R/Y5V: R_{ins} ≥ 500 MΩ or $R_{ins} \times C_r$ ≥ 25 seconds, whichever is less

Table 6 Test condition, procedure and requirements (continued)

TEST	TEST METHOD	PROCEDURE	REQUIREMENTS
Endurance	IEC 60384-21/22 4.14	Preconditioning; Initial measurements; after 150 +0/-10 °C for 1 hour, then keep for 24 ±1 hours at room temperature Duration and conditions: 1,000 ±12 hours at upper category temperature with 1.5 × U_r voltage applied Final measurement: perform a heat treatment at 150 +0/–10 °C for 1 hour, final measurements shall be carried out 24 ±1 hours after recovery at room temperature without load.	NP0: IΔC/CI: ≤ 2% or 1 pF whichever is greater X5R/X7R: IΔC/CI: ≤ 20% Y5V: IΔC/CI: ≤ 30% NP0/X5R/X7R/Y5V: D.F.: 2 × initial value max. NP0: R_{ins} ≥ 4,000 MΩ or R_{ins} × C_r ≥ 40 seconds, whichever is less X5R/X7R/Y5V: R_{ins} ≥ 1,000 MΩ or R_{ins} × C_r ≥ 50 seconds, whichever is less

REVISION HISTORY

REVISION	DATE	CHANGE NOTIFICATION	DESCRIPTION
Version 2	Apr 19, 2006	-	- New datasheet for ultra small NP0/X5R/X7R/Y5V series chip capacitors with lead-free terminations.