SN65LVDS10x 4-Port LVDS and 4-Port TTL-to-LVDS Repeaters

1 Features

- Receiver and Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard
  - SN65LVDS105 Receives Low-Voltage TTL (LVTTL) Levels
  - SN65LVDS104 Receives Differential Input Levels, ±100 mV
- Typical Data Signaling Rates to 400 Mbps or Clock Frequencies to 400 MHz
- Operates From a Single 3.3-V Supply
- Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load
- Propagation Delay Time
  - SN65LVDS105 – 2.2 ns (Typ)
  - SN65LVDS104 – 3.1 ns (Typ)
- LVTTL Levels Are 5-V Tolerant
- Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Networks
- Driver Outputs Are High-Impedance When Disabled or With V_{CC} <1.5 V
- Bus-Pin ESD Protection Exceeds 16 kV
- SOIC and TSSOP Packaging

2 Applications

- Clock Distribution
- Wireless Base Stations
- Network Routers

3 Description

The SN65LVDS10x are a differential line receiver and a LVTTL input (respectively) connected to four differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644 is a data signaling technique that offers low-power, low-noise coupling, and switching speeds to transmit data at relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. Having the drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

The SN65LVDS10x are characterized for operation from –40°C to 85°C.

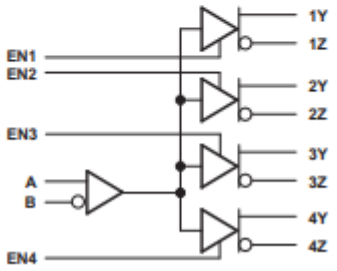
The SN65LVDS10x are members of a family of LVDS repeaters. A brief overview of the family is provided in the *Selection Guide to LVDS Repeaters* section.

Device Information[1]

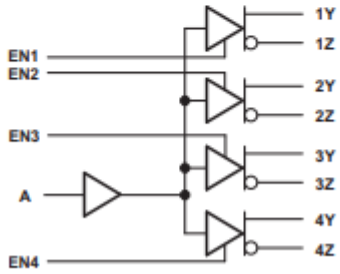
PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65LVDS104, SN65LVDS105	SOIC (16)	9.90 mm × 3.91 mm
	TSSOP (16)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

SN65LVDS104 Logic Diagram (Positive Logic)



SN65LVDS105 Logic Diagram (Positive Logic)

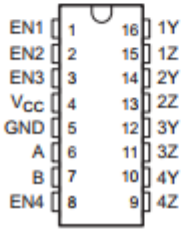


5 Selection Guide to LVDS Repeaters

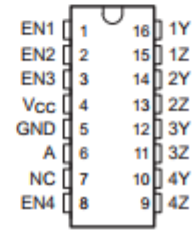
DEVICE	NO. INPUTS	NO. OUTPUTS	PACKAGE	COMMENT
SN65LVDS22	2 LVDS	2 LVDS	16-pin D	Dual multiplexed LVDS repeater
SN65LVDS104	1 LVDS	4 LVDS	16-pin D	4-Port LVDS repeater
SN65LVDS105	1 LVTTL	4 LVDS	16-pin D	4-Port TTL-to-LVDS repeater
SN65LVDS108	1 LVDS	8 LVDS	38-pin DBT	8-Port LVDS repeater
SN65LVDS109	2 LVDS	8 LVDS	38-pin DBT	Dual 4-port LVDS repeater
SN65LVDS116	1 LVDS	16 LVDS	64-pin DGG	16-Port LVDS repeater
SN65LVDS117	2 LVDS	16 LVDS	64-pin DGG	Dual 8-port LVDS repeater

6 Pin Configuration and Functions

SN65LVDS104 D or PW Package
16-Pin SOIC or TSSOP
Top View



SN65LVDS105 D or PW Package
16-Pin SOIC or TSSOP
Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	SN65LVDS104	SN65LVDS105		
A	6	6	I	LVDS input, positive (LVDS104) or LVTTL input, (LVDS105)
B	7	—	I	LVDS input, negative
EN1	1	1	I	Enable, channel 1
EN2	2	2	I	Enable, channel 2
EN3	3	3	I	Enable, channel 3
EN4	8	8	I	Enable, channel 4
GND	5	5	—	Ground
NC	—	7	—	No connect
V_{CC}	4	4	—	Supply voltage
1Y	16	16	O	LVDS output, positive, channel 1
1Z	15	15	O	LVDS output, negative, channel 1
2Y	14	14	O	LVDS output, positive, channel 2
2Z	13	13	O	LVDS output, negative, channel 2
3Y	12	12	O	LVDS output, positive, channel 3
3Z	11	11	O	LVDS output, negative, channel 3
4Y	10	10	O	LVDS output, positive, channel 4
4Z	9	9	O	LVDS output, negative, channel 4

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Supply voltage, V_{CC} (2)		–0.5	4	V
Voltage	Enables, A (SN65LVDS105)	–0.5	6	V
	A, B, Y or Z	–0.5	4	V
Continuous power dissipation		See *Dissipation Ratings*		
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds		260		°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings—JEDEC

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±12000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings—MIL-STD

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Tested in accordance with MIL-STD-883C Method 3015.7; A, B, Y, Z, and GND pins	Class 3, A	16000	V
			Class 3, B	400	

7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	3	3.3	3.6	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common-mode)	0		V_{CC}–0.8	
T_A	Operating free-air temperature	–40		85	°C

7.5 Thermal Information

THERMAL METRIC (1)		SN65LVDS104, SN65LVDS105 D (SOIC) 16 PINS	SN65LVDS104, SN65LVDS105 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.4	101.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.1	29.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	32	47.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6	1.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.7	46.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.6 SN65LVDS104 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP (1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	See Figure 13 and Table 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold	See Figure 13 and Table 1	–100			
$\lvert V_{OD}\rvert$	Differential output voltage magnitude	R_L = 100 Ω, V_{ID} = ± 100 mV, See Figure 13 and Figure 14	247	340	454	mV
$\Delta\lvert V_{OD}\rvert$	Change in differential output voltage magnitude between logic states	R_L = 100 Ω, V_{ID} = ± 100 mV, See Figure 13 and Figure 14	–50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 15	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 15	–50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 15		25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100 Ω		23	35	mA
		Disabled		3	8	
I_I	Input current (A or B inputs)	V_I = 0 V	–2	–11	–20	µA
		V_I = 2.4 V	–1.2	–3		
$I_{I(OFF)}$	Power-off Input current	V_{CC} = 1.5 V, V_I = 2.4 V			20	µA
I_{IH}	High-level input current (enables)	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current (enables)	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±10	mA
		V_{OD} = 0 V			±10	
I_{OZ}	High-impedance output current	V_O = 0 V or 2.4 V			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V			±1	µA
C_{IN}	Input capacitance (A or B inputs)	V_I = 0.4 sin (4E6πt) + 0.5 V		3		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

7.7 SN65LVDS105 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	R_L = 100 Ω, V_{ID} = ±100 mV, See Figure 18 and Figure 19	247	340	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states	R_L = 100 Ω, V_{ID} = ±100 mV, See Figure 18 and Figure 19	−50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 20	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states	See Figure 20	−50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See Figure 20		25	150	mV
I_{CC}	Supply current	Enabled, R_L = 100 Ω		23	35	mA
		Disabled		0.7	6.4	
I_{IH}	High-level input current	V_{IH} = 2 V			20	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V			10	µA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V			±10	mA
		V_{OD} = 0 V			±10	
I_{OZ}	High-impedance output current	V_O = 0 V or 2.4 V			±1	µA
$I_{O(OFF)}$	Power-off output current	V_{CC} = 1.5 V, V_O = 2.4 V		0.3	±1	µA
C_{IN}	Input capacitance	V_I = 0.4 sin (4E6πt) + 0.5 V		5		pF
C_O	Output capacitance (Y or Z outputs)	V_I = 0.4 sin (4E6πt) + 0.5 V, Disabled		9.4		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

7.8 SN65LVDS104 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 16	2.4	3.2	4.2	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 16	2.2	3.1	4.2	ns
t_r	Differential output signal rise time	R_L = 100 Ω, C_L = 10 pF, See Figure 16	0.3	0.8	1.2	ns
t_f	Differential output signal fall time	R_L = 100 Ω, C_L = 10 pF, See Figure 16	0.3	0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_L = 100 Ω, C_L = 10 pF, See Figure 16		150	500	ps
$t_{sk(o)}$	Channel-to-channel output skew(2)	R_L = 100 Ω, C_L = 10 pF, See Figure 16		20	100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 17		7.2	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 17		8.4	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 17		3.6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 17		6	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.9 SN65LVDS105 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 21	1.7	2.2	3	ns
t_{PHL}	Propagation delay time, high-to-low-level output	R_L = 100 Ω, C_L = 10 pF, See Figure 21	1.4	2.3	3.5	ns
t_r	Differential output signal rise time	R_L = 100 Ω, C_L = 10 pF, See Figure 21	0.3	0.8	1.2	ns
t_f	Differential output signal fall time	R_L = 100 Ω, C_L = 10 pF, See Figure 21	0.3	0.8	1.2	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	R_L = 100 Ω, C_L = 10 pF, See Figure 21		150	500	ps
$t_{sk(o)}$	Channel-to-channel output skew(2)	R_L = 100 Ω, C_L = 10 pF, See Figure 21		20	100	ps
$t_{sk(pp)}$	Part-to-part skew(3)				1.5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 22		7.2	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	See Figure 22		8.4	15	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 22		3.6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 22		6	15	ns

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the t_{PLH} or t_{PHL} of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.10 Dissipation Ratings

PACKAGE	$T_A \leq$ 25°C POWER RATING	OPERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 85°C POWER RATING
D	950 mW	7.6 mW/°C	494 mW
PW	774 mW	6.2 mW/°C	402 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

7.11 Typical Characteristics

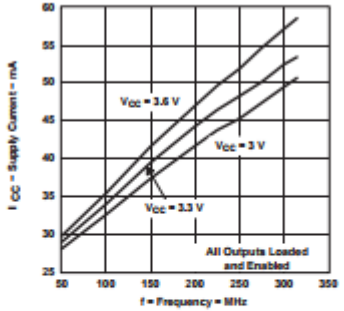


Figure 1. SN65LVDS104 Supply Current vs Frequency

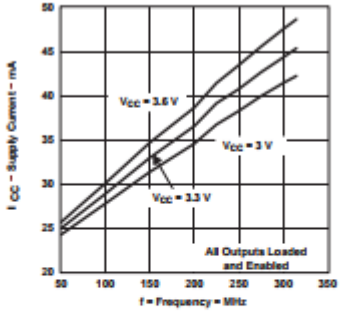


Figure 2. SN65LVDS105 Supply Current vs Frequency

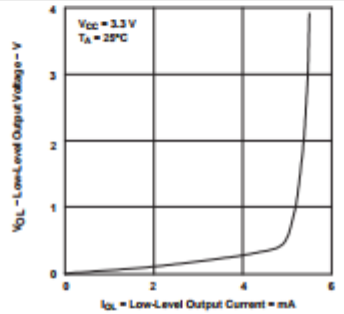


Figure 3. Driver Low-Level Output Voltage vs Low-Level Output Current

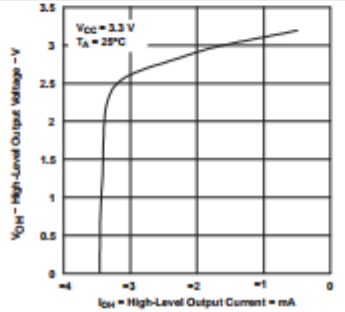


Figure 4. Driver High-Level Output Voltage vs High-Level Output Current

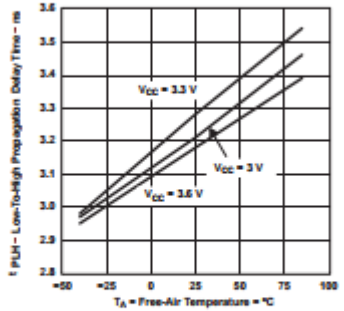


Figure 5. SN65LVDS104 Low-to-High Propagation Delay Time vs Free-Air Temperature

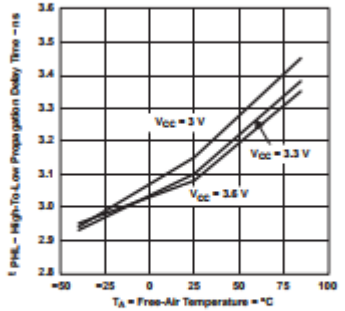


Figure 6. SN65LVDS104 High-to-Low Propagation Delay Time vs Free-Air Temperature

Typical Characteristics (continued)

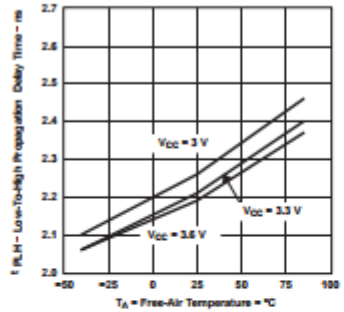


Figure 7. SN65LVDS105 Low-to-High Propagation Delay Time vs Free-Air Temperature

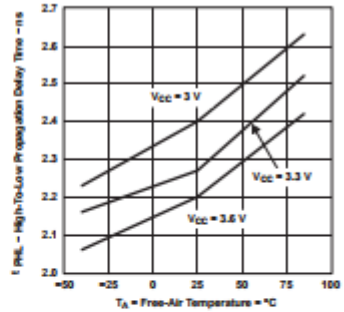
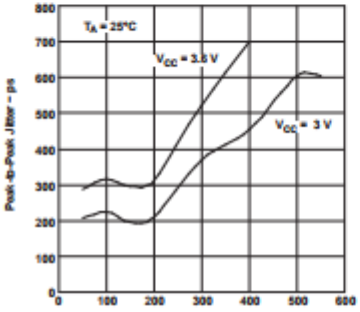
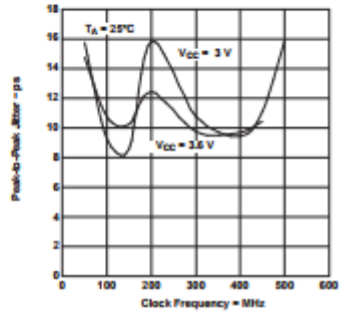


Figure 8. SN65LVDS105 High-to-Low Propagation Delay Time vs Free-Air Temperature



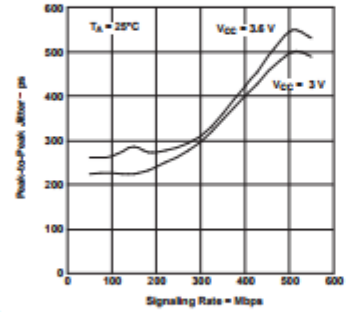
Input: 2^{15} PRBS with peak-to-peak jitter <115 ps at 100 Mbps. Test board adds about 70 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 9. SN65LVDS104 P-P Eye-Pattern Jitter vs PRBS Signaling Rate



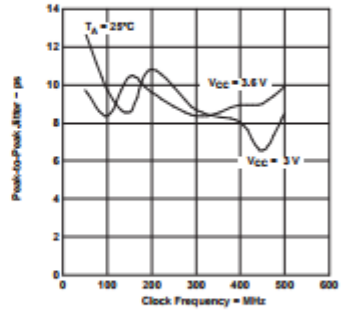
Input: 50% duty cycle square wave with period jitter < 9 ps at 100 MHz. Test board adds about 5 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 10. SN65LVDS104 P-P Period Jitter vs Clock Frequency



Input: 2^{15} PRBS with peak-to-peak Jitter < 147 ps at 100 Mbps, Test board adds about 43 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 11. SN65LVDS105 P-P Eye-Pattern Jitter vs PRBS Signaling Rate



Input: 50% duty cycle square wave with period jitter < 10 ps at 100 MHz. Test board adds about 5 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

Figure 12. SN65LVDS105 P-P Period Jitter vs Clock Frequency

8 Parameter Measurement Information

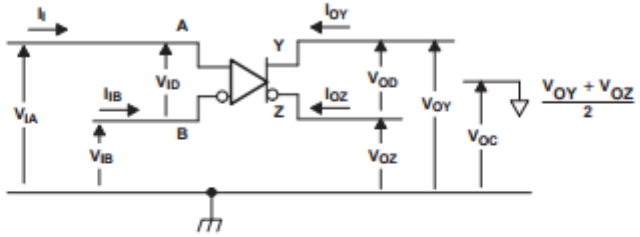


Figure 13. SN65LVDS104 Voltage and Current Definitions

Table 1. SN65LVDS104 Minimum and Maximum Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	–100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	–100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	–100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	–600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	–600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	–600 mV	0.3 V

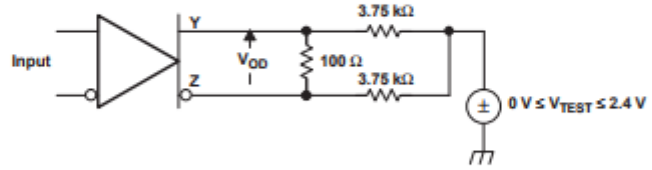
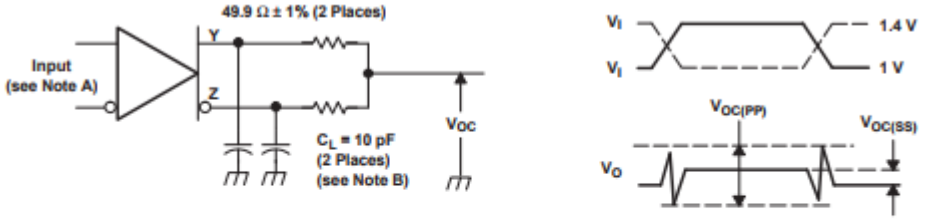


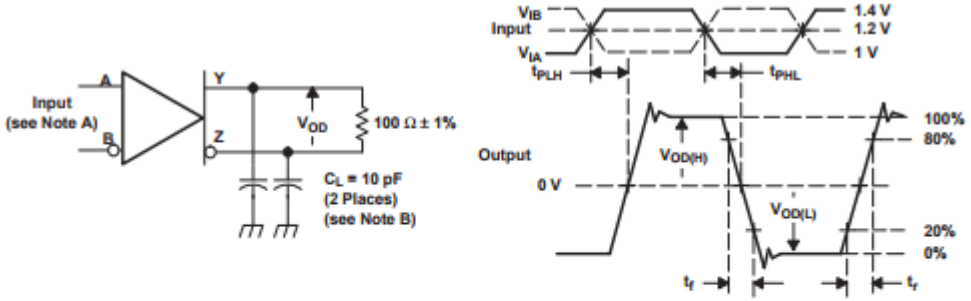
Figure 14. SN65LVDS104 V_{OD} Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

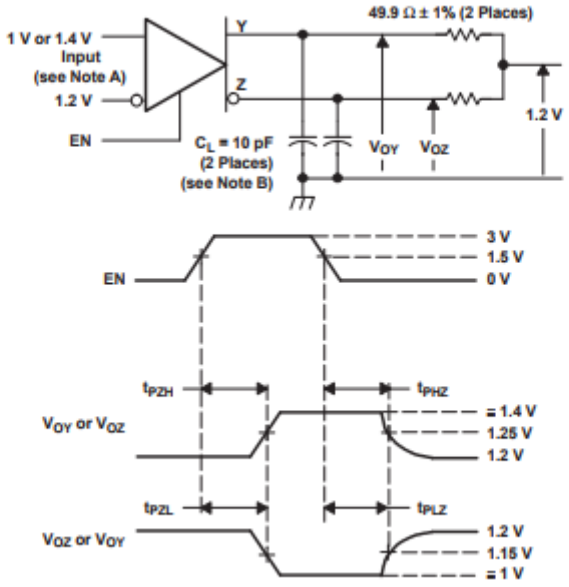
Figure 15. SN65LVDS104 Test Circuit and Definitions for the Driver Common-Mode Output Voltage



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 50 Mpps, and pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 16. SN65LVDS104 Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 17. SN65LVDS104 Enable and Disable Time Circuit and Definitions

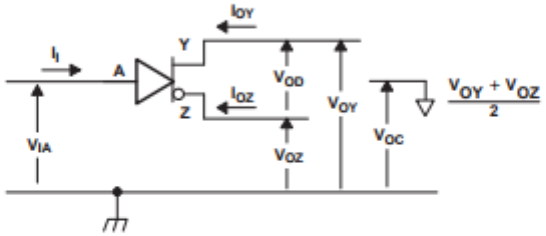


Figure 18. SN65LVDS105 Voltage and Current Definitions

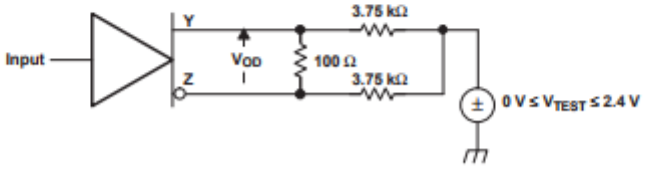
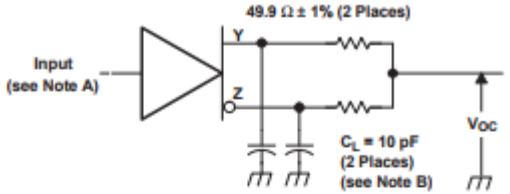
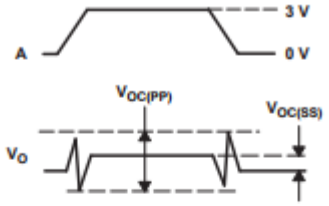


Figure 19. SN65LVDS105 VOD Test Circuit

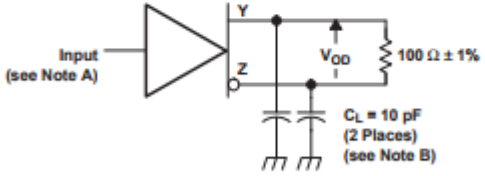


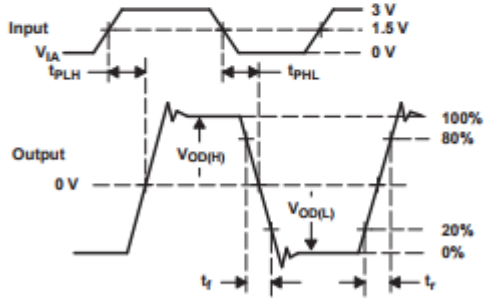


A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 0.5 Mpps, and pulse width = 500 ± 10 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

Figure 20. SN65LVDS105 Test Circuit and Definitions for the Driver Common-Mode Output Voltage





A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, Pulse Repetition Rate (PRR) = 50 Mpps, and pulse width = 10 ± 0.2 ns.

B. C_L includes instrumentation and fixture capacitance within 0.06 m of the device under test.

Figure 21. SN65LVDS105 Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal