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CYP15G0403DXB

Independent Clock Quad HOTLink II™ Transceiver

Features

- Second-generation HOTLink® technology
- Compliant to multiple standards
  - ESCON, DVB-ASI, Fibre Channel and Gigabit Ethernet (IEEE802.3z)
  - CPRI™ compliant
  - 8B/10B coded data or 10 bit uncoded data
- Quad channel transceiver operates from 195 to 1500 MBaud serial data rate
  - Aggregate throughput of up to 12 Gbits/second
- Second-generation HOTLink technology
- Truly independent channels
  - Each channel can operate at a different signaling rate
  - Each channel can transport a different type of data
- Selectable input/output clocking options
- Internal phase-locked loops (PLLs) with no external PLL components
- Dual differential PECL-compatible serial inputs per channel
- Internal DC-restoration
- Dual differential PECL-compatible serial outputs per channel
  - Source matched for 50-Ω transmission lines
  - No external bias resistors required
  - Signaling-rate controlled edge-rates
- MultiFrame™ Receive Framer provides alignment options
  - Bit and byte alignment
  - Comma or Full K28.5 detect
  - Single or Multi-byte Framer for byte alignment
  - Low-latency option
- Synchronous LVTTL parallel interface
- JTAG boundary scan
- Built-In Self-Test (BIST) for at-speed link testing
- Compatible with
  - Fiber-optic modules
  - Copper cables
  - Circuit board traces
- Per-channel Link Quality Indicator
  - Analog signal detect
  - Digital signal detect
- Low-power 3W at 3.3-V typical
- Single 3.3-V supply
- 256-ball thermally enhanced BGA
- Pb-free package option available
- 0.25 µ BiCMOS technology

Functional Description

The CYP15G0403DXB Independent Clock Quad HOTLink II™ Transceiver is a point-to-point or point-to-multi-point communications building block enabling transfer of data over a variety of high-speed serial links like optical fiber, balanced, and unbalanced copper transmission lines. The signaling rate can be anywhere in the range of 195 to 1500 MBaud per serial link. Each channel operates independently with its own reference clock allowing different rates. Each transmit channel accepts parallel characters in an Input Register, encodes each character for transport, and then converts it to serial data. Each receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to an Output Register. Figure 1 on page 2 illustrates typical connections between independent host systems and corresponding CYP15G0403DXB chips

As a second-generation HOTLink device, the CYP15G0403DXB extends the HOTLink family with enhanced levels of integration and faster data rates, while maintaining serial-link compatibility (data, command, and BIST) with other HOTLink devices. The transmit (TX) section of the CYP15G0403DXB Quad HOTLink II consists of four independent byte-wide channels. Each channel can accept either 8-bit data characters or preencoded 10-bit transmission characters. Data characters may be passed from the Transmit Input Register to an integrated 8B/10B Encoder to improve their serial transmission characteristics. These encoded characters are then serialized and output from dual Positive ECL (PECL) compatible differential transmission-line drivers at a bit-rate of either 10 or 20 times the input reference clock for that channel.

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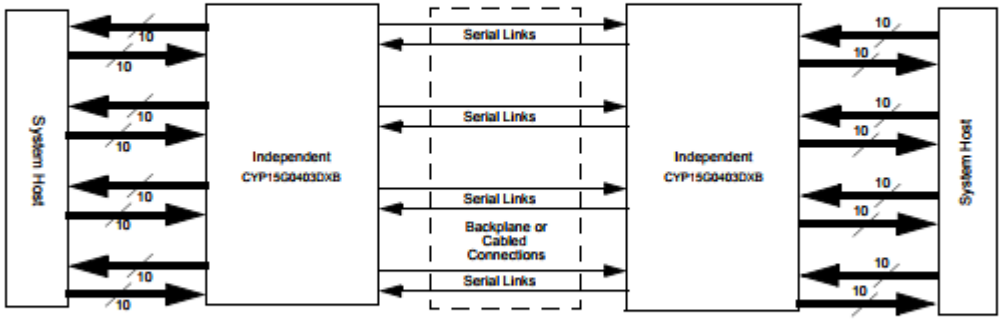
Figure 1. HOTLink II™ System Connections



The receive (RX) section of the CYP15G0403DXB Quad HOTLink II consists of four independent byte-wide channels. Each channel accepts a serial bit-stream from one of two PECL-compatible differential line receivers, and using a completely integrated Clock and Data Recovery PLL, recovers the timing information necessary for data reconstruction. Each recovered bit-stream is deserialized and framed into characters, 8B/10B decoded, and checked for transmission errors. Recovered decoded characters are then written to an internal Elasticity Buffer, and presented to the destination host system.

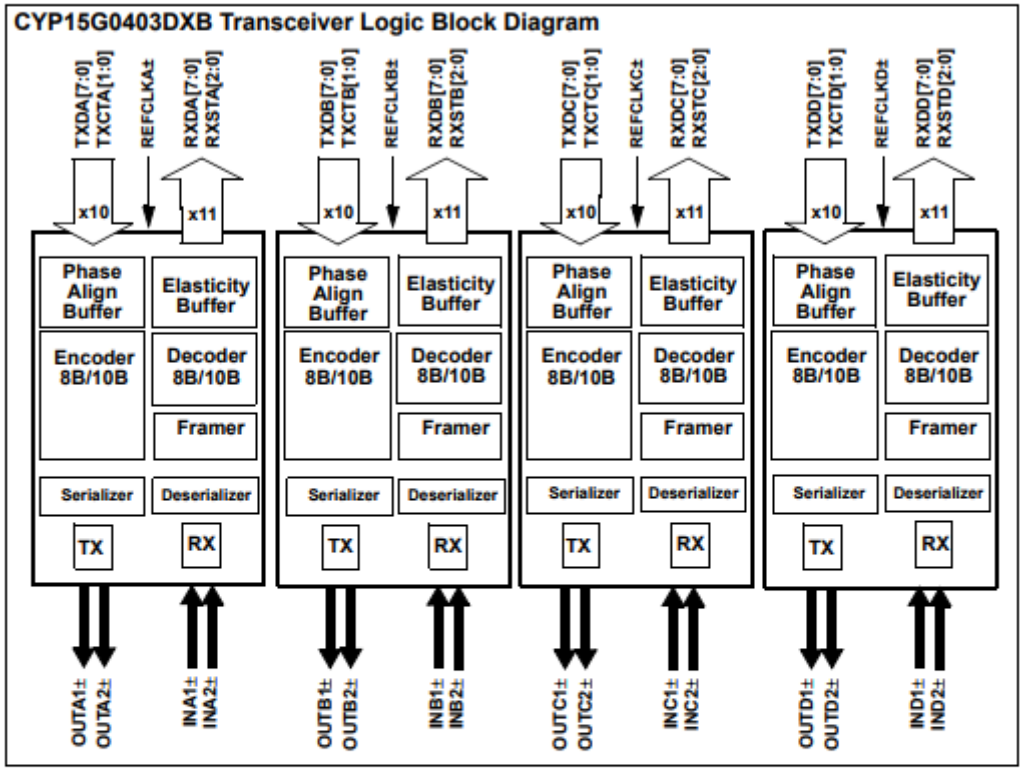
The integrated 8B/10B encoder/decoder may be bypassed for systems that present externally encoded or scrambled data at the parallel interface.

The parallel I/O interface may be configured for numerous forms of clocking to provide the highest flexibility in system architecture. In addition to clocking the transmit path with a local reference clock, the receive interface may also be configured to present data relative to a recovered clock or to a local reference clock.

Each transmit and receive channel contains an independent BIST pattern generator and checker. This BIST hardware allows at-speed testing of the high-speed serial data paths in each transmit and receive section, and across the interconnecting links.

The CYP15G0403DXB is ideal for port applications where different data rates and serial interface standards are necessary for each channel. Some applications include multi-protocol routers, aggregation equipment, and switches.

CYP15G0403DXB Transceiver Logic Block Diagram



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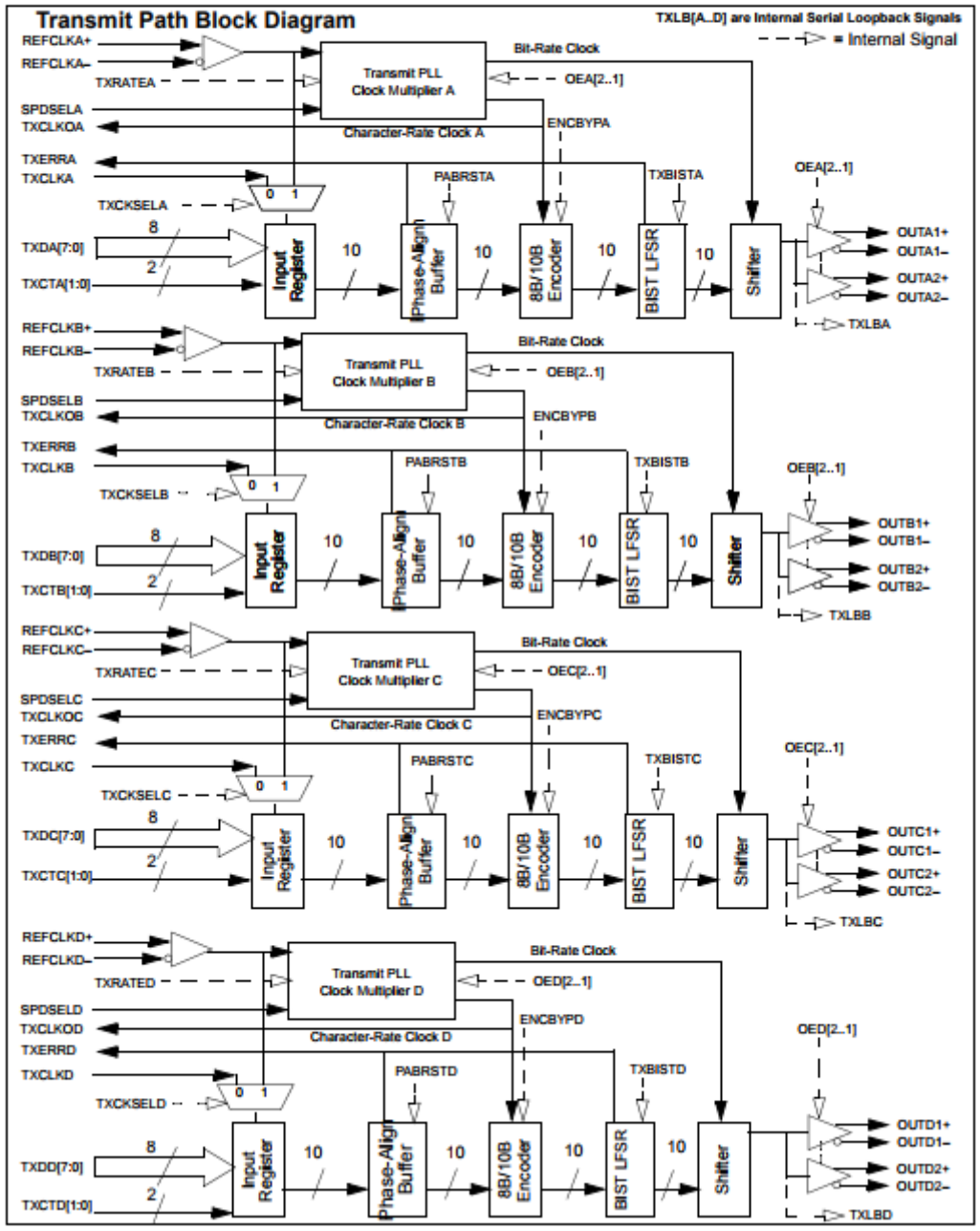
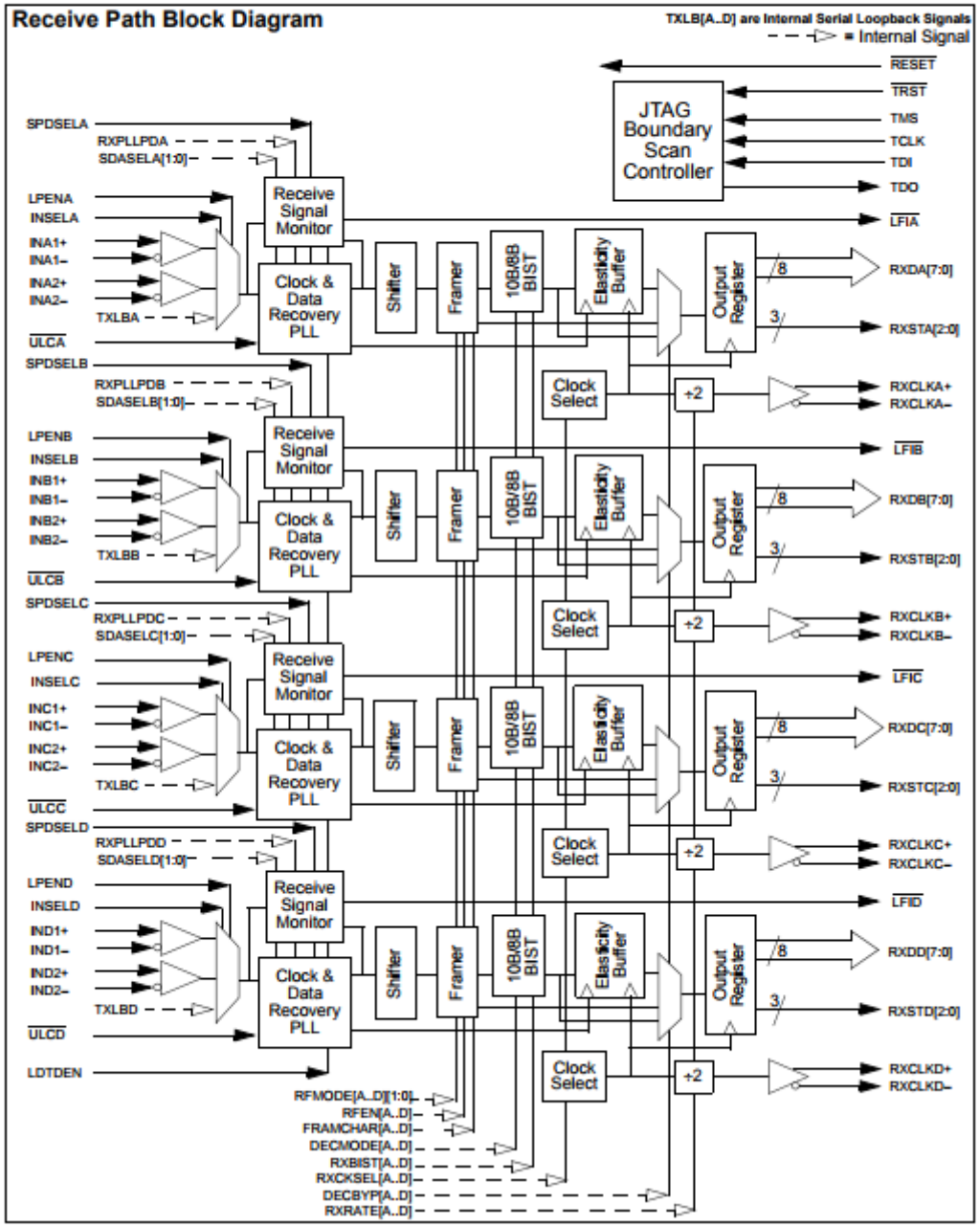
Transmit Path Block Diagram



Receive Path Block Diagram



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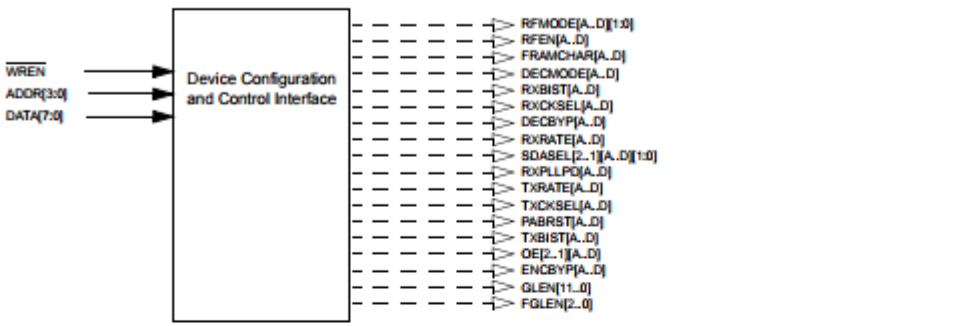
Device Configuration and Control Block Diagram



Pin Configuration (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	IN C1–	OUT C1–	IN C2–	OUT C2–	V_{CC}	IN D1–	OUT D1–	GND	IN D2–	OUT D2–	IN A1–	OUT A1–	GND	IN A2–	OUT A2–	V_{CC}	IN B1–	OUT B1–	IN B2–	OUT B2–
B	IN C1+	OUT C1+	IN C2+	OUT C2+	V_{CC}	IN D1+	OUT D1+	GND	IN D2+	OUT D2+	IN A1+	OUT A1+	GND	IN A2+	OUT A2+	V_{CC}	IN B1+	OUT B1+	IN B2+	OUT B2+
C	TDI	TMS	INSELC	INSELB	V_{CC}	$\overline{ULCD}$	$\overline{ULCC}$	GND	DATA [7]	DATA [5]	DATA [3]	DATA [1]	GND	NC	SPD SELD	V_{CC}	LDTD EN	$\overline{TRST}$	LPEND	TDO
D	TCLK	$\overline{RESET}$	INSELD	INSELA	V_{CC}	$\overline{ULCA}$	SPD SELC	GND	DATA [6]	DATA [4]	DATA [2]	DATA [0]	GND	LPENB	$\overline{ULCB}$	V_{CC}	LPENA	LTEN1	SCAN EN2	TMEN3
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	RX DC[6]	RX DC[7]	TX DC[0]	NC													NC	RX STB[1]	TX CLKOB	RX STB[0]
G	TX DC[7]	$\overline{WREN}$	TX DC[4]	TX DC[1]													SPD SELB	LP ENC	SPD SELA	RX DB[1]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	TX CTC[1]	TX DC[5]	TX DC[2]	TX DC[3]													RX STB[2]	RX DB[0]	RX DB[5]	RX DB[2]
K	RX DC[2]	REF CLKC–	TX CTC[0]	TX CLKC													RX DB[3]	RX DB[4]	RX DB[7]	$\overline{LFIB}$
L	RX DC[3]	REF CLKC+	$\overline{LFIC}$	TX DC[6]													RX DB[6]	RX CLKB+	RX CLKB–	TX DB[6]
M	RX DC[4]	RX DC[5]	NC	TX ERRC													REF CLKB+	REF CLKB–	TX ERRB	TX CLKB
N	GND	GND	GND	GND													GND	GND	GND	GND
P	RX DC[1]	RX DC[0]	RX STC[0]	RX STC[1]													TX DB[5]	TX DB[4]	TX DB[3]	TX DB[2]
R	RX STC[2]	TX CLKOC	RX CLKC+	RX CLKC–													TX DB[1]	TX DB[0]	TX CTB[1]	TX DB[7]
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	TX DD[0]	TX DD[1]	TX DD[2]	TX CTD[1]	V_{CC}	RX DD[2]	RX DD[1]	GND	TX CTA[1]	ADDR [0]	REF CLKD–	TX DA[1]	GND	TX DA[4]	TX CTA[0]	V_{CC}	RX DA[2]	TX CTB[0]	RX STA[2]	RX STA[1]
V	TX DD[3]	TX DD[4]	TX CTD[0]	RX DD[6]	V_{CC}	RX DD[3]	RX STD[0]	GND	RX STD[2]	ADDR [2]	REF CLKD+	TX CLKOA	GND	TX DA[3]	TX DA[7]	V_{CC}	RX DA[7]	RX DA[3]	RX DA[0]	RX STA[0]
W	TX DD[5]	TX DD[7]	$\overline{LFID}$	RX CLKD–	V_{CC}	RX DD[4]	RX STD[1]	GND	ADDR [3]	ADDR [1]	RX CLKA+	TX ERRA	GND	TX DA[2]	TX DA[6]	V_{CC}	$\overline{LFIA}$	REF CLKA+	RX DA[4]	RX DA[1]
Y	TX DD[6]	TX CLKD	RX DD[7]	RX CLKD+	V_{CC}	RX DD[5]	RX DD[0]	GND	TX CLKOD	NC	TX CLKA	RX CLKA–	GND	TX DA[0]	TX DA[5]	V_{CC}	TX ERRD	REF CLKA–	RX DA[6]	RX DA[5]

Pin Configuration (Bottom View)

	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	OUT B2–	IN B2–	OUT B1–	IN B1–	V_{CC}	OUT A2–	IN A2–	GND	OUT A1–	IN A1–	OUT D2–	IN D2–	GND	OUT D1–	IN D1–	V_{CC}	OUT C2–	IN C2–	OUT C1–	IN C1–
B	OUT B2+	IN B2+	OUT B1+	IN B1+	V_{CC}	OUT A2+	IN A2+	GND	OUT A1+	IN A1+	OUT D2+	IN D2+	GND	OUT D1+	IN D1+	V_{CC}	OUT C2+	IN 2+	OUT C1+	IN C1+
C	TDO	LP END	$\overline{TRST}$	LDTD EN	V_{CC}	SPD SELD	NC	GND	DATA [1]	DATA [3]	DATA [5]	DATA [7]	GND	$\overline{ULCC}$	$\overline{ULCD}$	V_{CC}	IN SELB	IN SELC	TMS	TDI
D	TMEN3	SCAN EN2	LTEN1	LP ENA	V_{CC}	$\overline{ULCB}$	LP ENB	GND	DATA [0]	DATA [2]	DATA [4]	DATA [6]	GND	SPD SELC	$\overline{ULCA}$	V_{CC}	IN SELA	IN SELD	$\overline{RESET}$	TCLK
E	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
F	RX STB[0]	TX CLKOB	RX STB[1]	NC													NC	TX DC[0]	RX DC[7]	RX DC[6]
G	RX DB[1]	SPD SELA	LP ENC	SPD SELB													TX DC[1]	TX DC[4]	$\overline{WREN}$	TX DC[7]
H	GND	GND	GND	GND													GND	GND	GND	GND
J	RX DB[2]	RX DB[5]	RX DB[0]	RX STB[2]													TX DC[3]	TX DC[2]	TX DC[5]	TX CTC[1]
K	$\overline{LFIB}$	RX DB[7]	RX DB[4]	RX DB[3]													TX CLKC	TX CTC[0]	REF CLKC–	RX DC[2]
L	TX DB[6]	RX CLKB–	RX CLKB+	RX DB[6]													TX DC[6]	$\overline{LFIC}$	REF CLKC+	RX DC[3]
M	TX CLKB	TX ERRB	REF CLKB–	REF CLKB+													TX ERRC	NC	RX DC[5]	RX DC[4]
N	GND	GND	GND	GND													GND	GND	GND	GND
P	TX DB[2]	TX DB[3]	TX DB[4]	TX DB[5]													RX STC[1]	RX STC[0]	RX DC[0]	RX DC[1]
R	TX DB[7]	TX CTB[1]	TX DB[0]	TX DB[1]													RX CLKC–	RX CLKC+	TX CLKOC	RX STC[2]
T	V_{CC}	V_{CC}	V_{CC}	V_{CC}													V_{CC}	V_{CC}	V_{CC}	V_{CC}
U	RX STA[1]	RX STA[2]	TX CTB[0]	RX DA[2]	V_{CC}	TX CTA[0]	TX DA[4]	GND	TX DA[1]	REF CLKD–	ADDR [0]	TXC TA[1]	GND	RX DD[1]	RX DD[2]	V_{CC}	TX CTD[1]	TX DD[2]	TX DD[1]	TX DD[0]
V	RX STA[0]	RX DA[0]	RX DA[3]	RX DA[7]	V_{CC}	TX DA[7]	TX DA[3]	GND	TX CLKOA	REF CLKD+	ADDR [2]	RX STD[2]	GND	RX STD[0]	RX DD[3]	V_{CC}	RX DD[6]	TX CTD[0]	TX DD[4]	TX DD[3]
W	RX DA[1]	RX DA[4]	REF CLKA+	$\overline{LFIA}$	V_{CC}	TX DA[6]	TX DA[2]	GND	TX ERRA	RX CLKA+	ADDR [1]	ADDR [3]	GND	RX STD[1]	RX DD[4]	V_{CC}	RX CLKD–	$\overline{LFID}$	TX DD[7]	TX DD[5]
Y	RX DA[5]	RX DA[6]	REF CLKA–	TX ERRD	V_{CC}	TX DA[5]	TX DA[0]	GND	RX CLKA–	TX CLKA	NC	TX CLKOD	GND	RX DD[0]	RX DD[5]	V_{CC}	RX CLKD+	RX DD[7]	TX CLKD	TX DD[6]

Pin Descriptions
CYP15G0403DXB Quad HOTLink II Transceiver

Name	I/O Characteristics	Signal Description
Transmit Path Data and Status Signals		
TXDA[7:0] TXDB[7:0] TXDC[7:0] TXDD[7:0]	LVTTL Input, synchronous, sampled by the associated TXCLKx↑ or REFCLKx↑[1]	**Transmit Data Inputs**. TXDx[7:0] data inputs are captured on the rising edge of the transmit interface clock. The transmit interface clock is selected by the TXCKSELx latch via the device configuration interface, and passed to the encoder or Transmit Shifter. When the Encoder is enabled, TXDx[7:0] specifies the specific data or command character sent.
TXCTA[1:0] TXCTB[1:0] TXCTC[1:0] TXCTD[1:0]	LVTTL Input, synchronous, sampled by the associated TXCLKx↑ or REFCLKx↑ [1]	**Transmit Control**. TXCTx[1:0] inputs are captured on the rising edge of the transmit interface clock. The transmit interface clock is selected by the TXCKSELx latch via the device configuration interface, and passed to the Encoder or Transmit Shifter. The TXCTA[1:0] inputs identify how the associated TXDx[7:0] characters are interpreted. When the Encoder is bypassed, these inputs are interpreted as data bits. When the Encoder is enabled, these inputs determine if the TXDx[7:0] character is encoded as Data, a Special Character code, or replaced with other Special Character codes. See Table 3 on page 16 for details.
TXERRA TXERRB TXERRC TXERRD	LVTTL Output, synchronous to REFCLKx↑ [2], synchronous to RXCLKx when selected as REFCLKx, asynchronous to transmit channel enable / disable, asynchronous to loss or return of REFCLKx±	**Transmit Path Error**. TXERRx is asserted HIGH to indicate detection of a transmit Phase-Align Buffer underflow or overflow. If an underflow or overflow condition is detected, TXERRx, for the channel in error, is asserted HIGH and remains asserted until either a Word Sync Sequence is transmitted on that channel, or the transmit Phase-Align Buffer is re-centered with the PABRSTx latch via the device configuration interface. When TXBISTx = 0, the BIST progress is presented on the associated TXERRx output. The TXERRx signal pulses HIGH for one transmit-character clock period to indicate a pass through the BIST sequence once every 511 or 527 (depending on RXCKSELx) character times. If RXCKSELx = 1, a one character pulse occurs every 527 character times. If RXCKSELx = 0, a one character pulse occurs every 511 character times. TXERRx is also asserted HIGH, when any of the following conditions is true: ■ The TXPLL for the associated channel is powered down. This occurs when OE2x and OE1x for a given channel are both disabled by setting OE2x = 0 and OE1x = 0. ■ The absence of the REFCLKx± signal
Transmit Path Clock Signals		
REFCLKA± REFCLKB± REFCLKC± REFCLKD±	Differential LVPECL or single-ended LVTTL input clock	**Reference Clock**. REFCLKx± clock inputs are used as the timing references for the transmit and receive PLLs. These input clocks may also be selected to clock the transmit and receive parallel interfaces. When driven by a single-ended LVCMOS or LVTTL clock source, connect the clock source to either the true or complement REFCLKx input, and leave the alternate REFCLKx input open (floating). When driven by an LVPECL clock source, the clock must be a differential clock, using both inputs.
TXCLKA TXCLKB TXCLKC TXCLKD	LVTTL Clock Input, internal pull-down	**Transmit Path Input Clock**. When configuration latch TXCKSELx = 0, the associated TXCLKx input is selected as the character-rate input clock for the TXDx[7:0] and TXCTx[1:0] inputs. In this mode, the TXCLKx input must be frequency-coherent to its associated TXCLKOx output clock, but may be offset in phase by any amount. Once initialized, TXCLKx is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKx drifts beyond the handling capacity of the Phase Align Buffer, TXERRx is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of the TXCLKx input clock relative to its associated REFCLKx± is initialized when the configuration latch PABRSTx is written as 0. When the associated TXERRx is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.

Notes
1. When REFCLKx± is configured for half-rate operation, these inputs are sampled relative to both the rising and falling edges of the associated REFCLKx±.
2. When REFCLKx± is configured for half-rate operation, these outputs are presented relative to both the rising and falling edges of the associated REFCLKx±.

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Pin Descriptions (continued)
CYP15G0403DXB Quad HOTLink II Transceiver

Name	I/O Characteristics	Signal Description
TXCLKOA TXCLKOB TXCLKOC TXCLKOD	LVTTL Output	**Transmit Clock Output**. TXCLKOx output clock is synthesized by each channel's transmit PLL and operates synchronous to the internal transmit character clock. TXCLKOx operates at either the same frequency as REFCLKx± (TXRATEx = 0), or at twice the frequency of REFCLKx± (TXRATEx = 1). The transmit clock outputs have no fixed phase relationship to REFCLKx±.
Receive Path Data and Status Signals		
RXDA[7:0] RXDB[7:0] RXDC[7:0] RXDD[7:0]	LVTTL Output, synchronous to the selected RXCLK± output or REFCLKx± input	**Parallel Data Output**. RXDx[7:0] parallel data outputs change relative to the receive interface clock. The receive interface clock is selected by the RXCKSELx latch. If RXCLKx± is a full-rate clock, the RXCLKx± clock outputs are complementary clocks operating at the character rate. The RXDx[7:0] outputs for the associated receive channels follow rising edge of RXCLKx+ or falling edge of RXCLKx–. If RXCLKx± is a half-rate clock, the RXCLKx± clock outputs are complementary clocks operating at half the character rate. The RXDx[7:0] outputs for the associated receive channels follow both the falling and rising edges of the associated RXCLKx± clock outputs.
RXSTA[2:0] RXSTB[2:0] RXSTC[2:0] RXSTD[2:0]	LVTTL Output, synchronous to the selected RXCLK± output or REFCLKx± input	**Parallel Status Output**. RXSTA[2:0] status outputs change relative to the receive interface clock. The receive interface clock is selected by the RXCKSELx latch. If RXCLKx± is a full-rate clock, the RXCLKx± clock outputs are complementary clocks operating at the character rate. The RXSTAx[2:0] outputs for the associated receive channels follow rising edge of RXCLKx+ or falling edge of RXCLKx–. If RXCLKx± is a half-rate clock, the RXCLKx± clock outputs are complementary clocks operating at half the character rate. The RXSTAx[2:0] outputs for the associated receive channels follow both the falling and rising edges of the associated RXCLKx± clock outputs. When the decoder is bypassed, RXSTx[1:0] become the two low-order bits of the 10-bit received character. RXSTx[2] = HIGH indicates the presence of a Comma character in the Output Register. When the decoder is enabled, RXSTx[2:0] provide status of the received signal. See Table 11 on page 28 for a list of received character status.
Receive Path Clock Signals		
RXCLKA± RXCLKB± RXCLKC± RXCLKD±	LVTTL Output Clock	**Receive Clock Output**. RXCLKx± is the receive interface clock used to control timing of the RXDx[7:0] and RXSTA[2:0] parallel outputs. The source of the RXCLKx± outputs is selected by the RXCKSELx latch via the device configuration interface. These true and complement clocks are used to control timing of data output transfers. These clocks are output continuously at either the dual-character rate (1/20th the serial bit-rate) or character rate (1/10th the serial bit-rate) of the data being received, as selected by RXRATEx. When configured such that the output data path is clocked by the REFCLKx± instead of a recovered clock, the RXCLKx± output drivers present a buffered or divided form (depending on RXRATEx) of the associated REFCLKx± that are delayed in phase to align with the data. This phase difference allows the user to select the optimal clock (REFCLKx± or RXCLK±) for setup/hold timing for their specific system. When REFCLKx± is a full-rate clock, the RXCLKx± rate depends on the value of RXRATEx. When REFCLKx± is a half-rate clock and RXCKSELx = 0, the RXCLKx± rate depends on the value of RXRATEx. When REFCLKx± is a half-rate clock and RXCKSELx=1, the RXCLKx± rate does not depend on the value of RXRATEx and operates at the same rate as REFCLKx±.

Pin Descriptions (continued)
CYP15G0403DXB Quad HOTLink II Transceiver

Name	I/O Characteristics	Signal Description
Device Control Signals		
RESET	LVTTL Input, asynchronous, internal pull-up	**Asynchronous Device Reset**. RESET initializes all state machines, counters, and configuration latches in the device to a known state. RESET must be asserted LOW for a minimum pulse width. When the reset is removed, all state machines, counters and configuration latches are at an initial state. As per the JTAG specifications the device RESET cannot reset the JTAG controller. Therefore, the JTAG controller has to be reset separately. Refer to "JTAG Support" on page 27 for the methods to reset the JTAG state machine. See Table 9 on page 22 for the initialize values of the device configuration latches.
LDTDEN	LVTTL Input, internal pull-up	**Level Detect Transition Density Enable**. When LDTDEN is HIGH, the Signal Level Detector, Range Controller, and Transition Density Detector are all enabled to determine if the RXPLL tracks REFCLKx± or the selected input serial data stream. If the Signal Level Detector, Range Controller, or Transition Density Detector are out of their respective limits while LDTDEN is HIGH, the RXPLL locks to REFCLK± until such a time they become valid. The (SDASEL[A..D][1:0]) are used to configure the trip level of the Signal Level Detector. The Transition Density Detector limit is one transition in every 60 consecutive bits. When LDTDEN is LOW, only the Range Controller is used to determine if the RXPLL tracks REFCLKx± or the selected input serial data stream. For the cases when RXCKSELx = 0 (recovered clock), it is recommended to set LDTDEN = HIGH.
ULCA ULCB ULCC ULCD	LVTTL Input, internal pull-up	**Use Local Clock**. When ULCx is LOW, the RXPLL is forced to lock to REFCLKx± instead of the received serial data stream. While ULCx is LOW, the LFIx for the associated channel is LOW indicating a link fault. When ULCx is HIGH, the RXPLL performs Clock and Data Recovery functions on the input data streams. This function is used in applications in which a stable RXCLKx± is needed. In cases when there is an absence of valid data transitions for a long period of time, or the high-gain differential serial inputs (INx±) are left floating, there may be brief frequency excursions of the RXCLKx± outputs from REFCLKx±.
SPDSELA SPDSELB SPDSELC SPDSELD	3-Level Select[3] static control input	**Serial Rate Select**. The SPDSELx inputs specify the operating signaling-rate range of each channel's transmit and receive PLL. LOW = 195 – 400 MBaud MID = 400 – 800 MBaud HIGH = 800 – 1500 MBaud
INSELA INSELB INSELC INSELD	LVTTL Input, asynchronous	**Receive Input Selector**. The INSELx input determines which external serial bit stream is passed to the receiver's Clock and Data Recovery circuit. When INSELx is HIGH, the Primary Differential Serial Data Input, INx1±, is selected for the associated receive channel. When INSELx is LOW, the Secondary Differential Serial Data Input, INx2±, is selected for the associated receive channel.
LPENA LPENB LPENC LPEND	LVTTL Input, asynchronous, internal pull-down	**Loop-Back-Enable**. The LPENx input enables the internal serial loop-back for the associated channel. When LPENx is HIGH, the transmit serial data from the associated channel is internally routed to the associated receive Clock and Data Recovery (CDR) circuit. All enabled serial drivers on the channel are forced to differential logic-1, and the serial data inputs are ignored. When LPENx is LOW, the internal serial loop-back function is disabled.

Note

3. 3-Level Select inputs are used for static configuration. These are ternary inputs that make use of logic levels of LOW, MID, and HIGH. The LOW level is usually implemented by direct connection to V_{SS} (ground). The HIGH level is usually implemented by direct connection to V_{CC} (power). The MID level is usually implemented by not connecting the input (left floating), which allows it to self bias to the proper level.

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Pin Descriptions (continued)
CYP15G0403DXB Quad HOTLink II Transceiver

Name	I/O Characteristics	Signal Description
LFIA LFIB LFIC LFID	LVTTL Output, asynchronous	**Link Fault Indication Output**. LFIx is an output status indicator signal. LFIx is the logical OR of six internal conditions. LFIx is asserted LOW when any of the following conditions is true: ■ Received serial data rate outside expected range ■ Analog amplitude below expected levels ■ Transition density lower than expected ■ Receive channel disabled ■ ULCx is LOW ■ Absence of REFCLKx±.
Device Configuration and Control Bus Signals		
WREN	LVTTL input, asynchronous, internal pull-up	**Control Write Enable**. The WREN input writes the values of the DATA[7:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[4]
ADDR[3:0]	LVTTL input asynchronous, internal pull-up	**Control Addressing Bus**. The ADDR[3:0] bus is the input address bus used to configure the device. The WREN input writes the values of the DATA[7:0] bus into the latch specified by the address location on the ADDR[3:0] bus.[4] Table 9 on page 22 lists the configuration latches within the device, and the initialization value of the latches upon the assertion of RESET. Table 10 on page 27 shows how the latches are mapped in the device.
DATA[7:0]	LVTTL input asynchronous, internal pull-up	**Control Data Bus**. The DATA[7:0] bus is the input data bus used to configure the device. The WREN input writes the values of the DATA[7:0] bus into the latch specified by address location on the ADDR[3:0] bus.[4] Table 9 lists the configuration latches within the device, and the initialization value of the latches upon the assertion of RESET. Table 10 shows how the latches are mapped in the device.
Internal Device Configuration Latches		
RFMODE[A..D][1:0]	Internal Latch[5]	**Reframe Mode Select**.
FRAMCHAR[A..D]	Internal Latch[5]	**Framing Character Select**.
DECMODE[A..D]	Internal Latch[5]	**Receiver Decoder Mode Select**.
DECBYP[A..D]	Internal Latch[5]	**Receiver Decoder Bypass**.
RXCKSEL[A..D]	Internal Latch[5]	**Receive Clock Select**.
RXRATE[A..D]	Internal Latch[5]	**Receive Clock Rate Select**.
SDASEL[A..D][1:0]	Internal Latch[5]	**Signal Detect Amplitude Select**.
ENCBYP[A..D]	Internal Latch[5]	**Transmit Encoder Bypassed**.
TXCKSEL[A..D]	Internal Latch[5]	**Transmit Clock Select**.
TXRATE[A..D]	Internal Latch[5]	**Transmit PLL Clock Rate Select**.
RFEN[A..D]	Internal Latch[5]	**Reframe Enable**.
RXPLLPD[A..D]	Internal Latch[5]	**Receive Channel Power Control**.
RXBIST[A..D]	Internal Latch[5]	**Receive Bist Disabled**.
TXBIST[A..D]	Internal Latch[5]	**Transmit Bist Disabled**.
OE2[A..D]	Internal Latch[5]	**Differential Serial Output Driver 2 Enable**.
OE1[A..D]	Internal Latch[5]	**Differential Serial Output Driver 1 Enable**.

Notes

4. See "Device Configuration and Control Interface" on page 22 for detailed information on the operation of the Configuration Interface.
5. See "Device Configuration and Control Interface" on page 22 for detailed information on the internal latches.

Pin Descriptions (continued)
CYP15G0403DXB Quad HOTLink II Transceiver

Name	I/O Characteristics	Signal Description
PABRST[A..D]	Internal Latch[5]	**Transmit Clock Phase Alignment Buffer Reset.**
GLEN[11..0]	Internal Latch[5]	**Global Latch Enable.**
FGLEN[2..0]	Internal Latch[5]	**Force Global Latch Enable.**
Factory Test Modes		
LTEN1	LVTTL input, internal pull-down	**Factory Test 1.** LTEN1 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
SCANEN2	LVTTL input, internal pull-down	**Factory Test 2.** SCANEN2 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
TMEN3	LVTTL input, internal pull-down	**Factory Test 3.** TMEN3 input is for factory testing only. This input may be left as a NO CONNECT, or GND only.
Analog I/O		
OUTA1± OUTB1± OUTC1± OUTD1±	CML Differential Output	**Primary Differential Serial Data Output.** The OUTx1± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
OUTA2± OUTB2± OUTC2± OUTD2±	CML Differential Output	**Secondary Differential Serial Data Output.** The OUTx2± PECL-compatible CML outputs (+3.3V referenced) are capable of driving terminated transmission lines or standard fiber-optic transmitter modules, and must be AC-coupled for PECL-compatible connections.
INA1± INB1± INC1± IND1±	Differential Input	**Primary Differential Serial Data Input.** The INx1± input accepts the serial data stream for deserialization and decoding. The INx1± serial stream is passed to the receive CDR circuit to extract the data content when INSELx = HIGH.
INA2± INB2± INC2± IND2±	Differential Input	**Secondary Differential Serial Data Input.** The INx2± input accepts the serial data stream for deserialization and decoding. The INx2± serial stream is passed to the receiver CDR circuit to extract the data content when INSELx = LOW.
JTAG Interface		
TMS	LVTTL Input, internal pull-up	**Test Mode Select.** Used to control access to the JTAG Test Modes. If maintained high for ≥5 TCLK cycles, the JTAG test controller is reset.
TCLK	LVTTL Input, internal pull-down	**JTAG Test Clock.**
TDO	3-State LVTTL Output	**Test Data Out.** JTAG data output buffer. High-Z while JTAG test mode is not selected.
TDI	LVTTL Input, internal pull-up	**Test Data In.** JTAG data input port.
$\overline{\text{TRST}}$	LVTTL Input, internal pull-up	**JTAG reset signal.** When asserted (LOW), this input asynchronously resets the JTAG test access port controller.
Power		
V_{CC}		**+3.3V Power.**
GND		**Signal and Power Ground for all internal circuits.**

CYP15G0403DXB

CYP15G0403DXB HOTLink II Operation

The CYP15G0403DXB is a highly configurable, independent clocking, quad-channel transceiver designed to support reliable transfer of large quantities of data, using high-speed serial links from multiple sources to multiple destinations. This device supports four single-byte channels.

CYP15G0403DXB Transmit Data Path

Input Register

The bits in the Input Register for each channel support different assignments, based on if the input data is encoded or unencoded. These assignments are shown in Table 1.

When the ENCODER is enabled, each input register captures eight data bits and two control bits on each input clock cycle. When the Encoder is bypassed, the control bits are part of the pre-encoded 10-bit character.

When the Encoder is enabled, the TXCTx[1:0] bits are interpreted along with the associated TXDx[7:0] character to generate a specific 10-bit transmission character.

Phase-Align Buffer

Data from each Input Register is passed to the associated Phase-Align Buffer, when the TXDx[7:0] and TXCTx[1:0] input registers are clocked using TXCLKx‡ (TXCKSELx = 0 and TXRATEx = 0). When the TXDx[7:0] and TXCTx[1:0] input registers are clocked using REFCLKx± (TXCKSELx = 1) and REFCLKx± is a full-rate clock, the associated Phase Alignment Buffer in the transmit path is bypassed. These buffers are used to absorb clock phase differences between the TXCLKx input clock and the internal character clock for that channel.

Once initialized, TXCLKx is allowed to drift in phase as much as ±180 degrees. If the input phase of TXCLKx drifts beyond the handling capacity of the Phase Align Buffer, TXERRx is asserted to indicate the loss of data, and remains asserted until the Phase Align Buffer is initialized. The phase of the TXCLKx relative to its associated internal character rate clock is initialized when the configuration latch PABRSTx is written as 0. When the associated TXERRx is deasserted, the Phase Align Buffer is initialized and input characters are correctly captured.

Table 1. Input Register Bit Assignments[6]

Signal Name	Unencoded	Encoded
TXDx[0] (LSB)	DINx[0]	TXDx[0]
TXDx[1]	DINx[1]	TXDx[1]
TXDx[2]	DINx[2]	TXDx[2]
TXDx[3]	DINx[3]	TXDx[3]
TXDx[4]	DINx[4]	TXDx[4]
TXDx[5]	DINx[5]	TXDx[5]
TXDx[6]	DINx[6]	TXDx[6]
TXDx[7]	DINx[7]	TXDx[7]
TXCTx[0]	DINx[8]	TXCTx[0]
TXCTx[1] (MSB)	DINx[9]	TXCTx[1]

If the phase offset, between the initialized location of the input clock and REFCLKx‡, exceeds the skew handling capabilities of the Phase-Align Buffer, an error is reported on that channel's TXERRx output. This output indicates an error continuously until the Phase-Align Buffer for that channel is reset. While the error remains active, the transmitter for that channel outputs a continuous C0.7 character to indicate to the remote receiver that an error condition is present in the link.

Each Phase-Align Buffer may be individually reset with minimal disruption of the serial data stream. When a Phase-Align Buffer error is present, the transmission of a Word Sync Sequence re-centers the Phase-Align Buffer and clears the error indication.

Note. K28.5 characters may be added or removed from the data stream during the Phase Align Buffer reset operation. When used with non-Cypress devices that require a complete 16-character Word Sync Sequence for proper receive Elasticity Buffer Operation, it is recommend that the Phase Alignment Buffer reset be followed by a Word Sync Sequence to ensure proper operation.

Encoder

Each character received from the Input Register or Phase-Align Buffer is passed to the Encoder logic. This block interprets each character and any associated control bits, and outputs a 10-bit transmission character.

Depending on the operational mode, the generated transmission character may be

- the 10-bit pre-encoded character accepted in the Input Register.
- the 10-bit equivalent of the 8-bit Data character accepted in the Input Register.
- the 10-bit equivalent of the 8-bit Special Character code accepted in the Input Register.
- the 10-bit equivalent of the C0.7 violation character if a Phase-Align Buffer overflow or underflow error is present.
- a character that is part of the 511-character BIST sequence.
- a K28.5 character generated as an individual character or as part of the 16-character Word Sync Sequence.

Data Encoding

Raw data, as received directly from the Transmit Input Register, is seldom in a form suitable for transmission across a serial link. The characters must usually be processed or transformed to guarantee

- a minimum transition density (to allow the receive PLL to extract a clock from the serial data stream).
- a DC-balance in the signaling (to prevent baseline wander).
- run-length limits in the serial data (to limit the bandwidth requirements of the serial link).
- the remote receiver a way of determining the correct character boundaries (framing).

When the Encoder is enabled (ENCBYPx = 1), the characters transmitted are converted from Data or Special Character codes to 10-bit transmission characters, using an integrated 8B/10B encoder. When directed to encode the character as a Special Character code, the encoder uses the Special Character encoding rules listed in Table 16 on page 46. When directed to encode the character as a Data character, it is encoded using the Data Character encoding rules in Table 15 on page 42.

The 8B/10B encoder is standards compliant with ANSI/NCITS ASC X3.230-1994 Fibre Channel, IEEE 802.3z Gigabit Ethernet, the IBM® ESCON® and FICON™ channels, ETSI DVB-ASI, and ATM Forum standards for data transport.

Many of the Special Character codes listed in Table 16 may be generated by more than one input character. The CYP15G0403DXB is designed to support two independent (but non-overlapping) Special Character code tables. This allows the CYP15G0403DXB to operate in mixed environments with other Cypress HOTLink devices using the enhanced Cypress command code set, and the reduced command sets of other non-Cypress devices. Even when used in an environment that normally uses non-Cypress Special Character codes, the selective use of Cypress command codes can permit operation where running disparity and error handling must be managed.

Following conversion of each input character from eight bits to a 10-bit transmission character, it is passed to the Transmit Shifter and is shifted out LSB first, as required by ANSI and IEEE standards for 8B/10B coded serial data streams.

Transmit Modes

Encoder Bypass

When the Encoder is bypassed, the character captured from the TXDx[7:0] and TXCTx[1:0] input register is passed directly to the transmit shifter without modification. With the encoder bypassed, the TXCTx[1:0] inputs are considered part of the data character and do not perform a control function that would otherwise modify the interpretation of the TXDx[7:0] bits. The bit usage and mapping of these control bits when the Encoder is bypassed is shown in Table 2.

Table 2. Encoder Bypass Mode

Signal Name	Bus Weight	10B Name
TXDx[0] (LSB)	2^0	a[6]
TXDx[1]	2^1	b
TXDx[2]	2^2	c
TXDx[3]	2^3	d
TXDx[4]	2^4	e
TXDx[5]	2^5	i
TXDx[6]	2^6	f
TXDx[7]	2^7	g
TXCTx[0]	2^8	h
TXCTx[1] (MSB)	2^9	j

When the encoder is enabled, the TXCTx[1:0] data control bits control the interpretation of the TXDx[7:0] bits and the characters generated by them. These bits are interpreted as listed in Table 3.

Table 3. Transmit Modes

TXCTx[1]	TXCTx[0]	Characters Generated
0	0	Encoded data character
0	1	K28.5 fill character
1	0	Special character code
1	1	16-character Word Sync Sequence

Word Sync Sequence

When TXCTx[1:0] = 11, a 16-character sequence of K28.5 characters, known as a Word Sync Sequence, is generated on the associated channel. This sequence of K28.5 characters may start with either a positive or negative disparity K28.5 (as determined by the current running disparity and the 8B/10B coding rules). The disparity of the second and third K28.5 characters in this sequence are reversed from what normal 8B/10B coding rules would generate. The remaining K28.5 characters in the sequence follow all 8B/10B coding rules. The disparity of the generated K28.5 characters in this sequence follow a pattern of either ++−−+−+−+−+−+− or −−++−+−+−+−+−+.

The generation of this sequence, once started, cannot be stopped until all 16 characters have been sent. The content of the associated input registers are ignored for the duration of this sequence. At the end of this sequence, if the TXCTx[1:0] = 11 condition is sampled again, the sequence restarts and remains uninterruptible for the following 15 character clocks.

Transmit BIST

Each transmit channel contains an internal pattern generator that can be used to validate both the link and device operation. These generators are enabled by the associated TXBISTx latch via the device configuration interface. When enabled, a register in the associated transmit channel becomes a signature pattern generator by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character (or 526-character) sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Receiver(s).

A device reset ($\overline{\text{RESET}}$ sampled LOW) presets the BIST Enable Latches to disable BIST on all channels.

All data and data-control information present at the associated TXDx[7:0] and TXCTx[1:0] inputs are ignored when BIST is active on that channel. If the receive channels are configured for reference clock operation, each pass is preceded by a 16-character Word Sync Sequence to allow Elasticity Buffer alignment and management of clock-frequency variations.

Transmit PLL Clock Multiplier

Each Transmit PLL Clock Multiplier accepts a character-rate or half-character-rate external clock at the associated REFCLKx± input, and that clock is multiplied by 10 or 20 (as selected by TXRATEx) to generate a bit-rate clock for use by the transmit shifter. It also provides a character-rate clock used by the transmit paths, and outputs this character rate clock as TXCLKOx.

Each clock multiplier PLL can accept a REFCLKx± input between 19.5 MHz and 150 MHz, however, this clock range is limited by the operating mode of the CYP15G0403DXB clock multiplier (TXRATEx) and by the level on the associated SPDSELx input.

SPDSELx are 3-level select[3] inputs that select one of three operating ranges for the serial data outputs and inputs of the associated channel. The operating serial signaling-rate and allowable range of REFCLKx± frequencies are listed in Table 4.

Table 4. Operating Speed Settings

SPDSELx	TXRATE	REFCLKx± Frequency (MHz)	Signaling Rate (MBaud)
LOW	1	reserved	195–400
	0	19.5–40	
MID (Open)	1	20–40	400–800
	0	40–80	
HIGH	1	40–75	800–1500
	0	80–150	

The REFCLKx± inputs are differential inputs with each input internally biased to 1.4V. If the REFCLKx+ input is connected to a TTL, LVTTL, or LVCMOS clock source, the input signal is recognized when it passes through the internally biased reference point. When driven by a single-ended TTL, LVTTL, or LVCMOS clock source, connect the clock source to either the true or complement REFCLKx input, and leave the alternate REFCLKx input open (floating).

When both the REFCLKx+ and REFCLKx– inputs are connected, the clock source must be a differential clock. This can either be a differential LVPECL clock that is DC-or AC-coupled or a differential LVTTL or LVCMOS clock.

By connecting the REFCLKx– input to an external voltage source, it is possible to adjust the reference point of the REFCLKx+ input for alternate logic levels. When doing so it is necessary to ensure that the input differential crossing point remains within the parametric range supported by the input.

Serial Output Drivers

The serial output interface drivers use differential Current Mode Logic (CML) drivers to provide source-matched drivers for transmission lines. These drivers accept data from the Transmit Shifters. These drivers have signal swings equivalent to that of standard PECL drivers, and are capable of driving AC-coupled optical modules or transmission lines. When configured for local loopback (LPENx = HIGH), all enabled serial drivers are configured to drive a static differential logic.

Transmit Channels Enabled

Each driver can be enabled or disabled separately via the device configuration interface.

When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down. A device reset ($\overline{\text{RESET}}$ sampled LOW) disables all output drivers.

Note. When a disabled transmit channel (i.e., both outputs disabled) is re-enabled:

- data on the serial outputs may not meet all timing specifications for up to 250 µs
- the state of the phase-align buffer cannot be guaranteed, and a phase-align reset is required if the phase-align buffer is used

CYP15G0403DXB Receive Data Path

Serial Line Receivers

Two differential Line Receivers, INx1± and INx2±, are available on each channel for accepting serial data streams. The active Serial Line Receiver on a channel is selected using the associated INSELx input. The Serial Line Receiver inputs are differential, and can accommodate wire interconnect and filtering losses or transmission line attenuation greater than 16 dB. For normal operation, these inputs should receive a signal of at least VI_{DIFF} > 100 mV, or 200 mV peak-to-peak differential. Each Line Receiver can be DC- or AC-coupled to +3.3V powered fiber-optic interface modules (any ECL/PECL family, not limited to 100K PECL) or AC-coupled to +5V powered optical modules. The common-mode tolerance of these line receivers accommodates a wide range of signal termination voltages. Each receiver provides internal DC-restoration, to the center of the receiver's common mode range, for AC-coupled signals.

The local internal loopback (LPENx) allows the serial transmit data outputs to be routed internally back to the Clock and Data Recovery circuit associated with each channel. When configured for local loopback, the associated transmit serial driver outputs are forced to output a differential logic-1. This prevents local diagnostic patterns from being broadcast to attached remote receivers.

Signal Detect/Link Fault

Each selected Line Receiver (i.e., that routed to the clock and data recovery PLL) is simultaneously monitored for

- analog amplitude above amplitude level selected by SDASELx
- transition density above the specified limit
- range controls report the received data stream inside normal frequency range (±1500 ppm[27])
- receive channel enabled
- Presence of reference clock
- $\overline{\text{ULCx}}$ is not asserted.

All of these conditions must be valid for the Signal Detect block to indicate a valid signal is present. This status is presented on the LFIx (Link Fault Indicator) output associated with each receive channel, which changes synchronous to the selected receive interface clock.

Analog Amplitude

While most signal monitors are based on fixed constants, the analog amplitude level detection is adjustable to allow operation with highly attenuated signals, or in high-noise environments. The analog amplitude level detection is set by the SDASELx

latch via device configuration interface. The SDASELx latch sets the trip point for the detection of a valid signal at one of three levels, as listed in Table 5. This control input affects the analog monitors for all receive channels.

Table 5. Analog Amplitude Detect Valid Signal Levels[7]

SDASEL	Typical Signal with Peak Amplitudes Above
00	Analog Signal Detector is disabled
01	140 mV p-p differential
10	280 mV p-p differential
11	420 mV p-p differential

The Analog Signal Detect monitors are active for the Line Receiver as selected by the associated INSELx input. When configured for local loopback, no input receivers are selected, and the LFIx output for each channel reports only the receive VCO frequency out-of-range and transition density status of the associated transmit signal. When local loopback is active, the associated Analog Signal Detect Monitor is disabled.

Transition Density

The Transition Detection logic checks for the absence of transitions spanning greater than six transmission characters (60 bits). If no transitions are present in the data received, the Detection logic for that channel asserts LFIx.

Range Controls

The CDR circuit includes logic to monitor the frequency of the PLL Voltage Controlled Oscillator (VCO) used to sample the incoming data stream. This logic ensures that the VCO operates at, or near the rate of the incoming data stream for two primary cases:

- when the incoming data stream resumes after a time in which it has been "missing."
- when the incoming data stream is outside the acceptable signaling rate range.

To perform this function, the frequency of the RXPLL VCO is periodically compared to the frequency of the REFCLKx± input. If the VCO is running at a frequency beyond ±1500 ppm[27] as defined by the REFCLKx± frequency, it is periodically forced to the correct frequency (as defined by REFCLKx±, SPDSELx, and TXRATEx) and then released in an attempt to lock to the input data stream.

The sampling and relock period of the Range Control is calculated as follows: RANGE_CONTROL_ SAMPLING_PERIOD = (RECOVERED BYTE CLOCK PERIOD) * (4096).

During the time that the Range Control forces the RXPLL VCO to track REFCLKx±, the LFIx output is asserted LOW. After a valid serial data stream is applied, it may take up to one RANGE CONTROL SAMPLING PERIOD before the PLL locks to the input data stream, after which LFIx should be HIGH.

Receive Channel Enabled

The CYP15G0403DXB contains four receive channels that can be independently enabled and disabled. Each channel can be enabled or disabled separately through the RXPLLPDx input latch as controlled by the device configuration interface. When the RXPLLPDx latch = 0, the associated PLL and analog circuitry of the channel is disabled. Any disabled channel indicates a constant link fault condition on the LFIx output. When RXPLLPDx = 1, the associated PLL and receive channel is enabled to receive and decode a serial stream.

Note. When a disabled receive channel is reenabled, the status of the associated LFIx output and data on the parallel outputs for the associated channel may be indeterminate for up to 2 ms.

Clock/Data Recovery

The extraction of a bit-rate clock and recovery of bits from each received serial stream is performed by a separate CDR block within each receive channel. The clock extraction function is performed by an integrated PLL that tracks the frequency of the transitions in the incoming bit stream and align the phase of the internal bit-rate clock to the transitions in the selected serial data stream.

Each CDR accepts a character-rate (bit-rate ÷ 10) or half-character-rate (bit-rate ÷ 20) reference clock from the associated REFCLKx± input. This REFCLKx± input is used to

- ensure that the VCO (within the CDR) is operating at the correct frequency (rather than a harmonic of the bit-rate)
- reduce PLL acquisition time
- limit unlocked frequency excursions of the CDR VCO when there is no input data present at the selected Serial Line Receiver.

Regardless of the type of signal present, the CDR attempts to recover a data stream from it. If the signalling rate of the recovered data stream is outside the limits set by the range control monitors, the CDR tracks REFCLKx± instead of the data stream. Once the CDR output (RXCLK±) frequency returns back close to REFCLKx± frequency, the CDR input is switched back to the input data stream. If no data is present at the selected line receiver, this switching behavior may result in brief RXCLK± frequency excursions from REFCLKx±. However, the validity of the input data stream is indicated by the LFIx output. The frequency of REFCLKx± is required to be within ±1500 ppm[27] of the frequency of the clock that drives the REFCLKx± input of the *remote* transmitter to ensure a lock to the incoming data stream.

For systems using multiple or redundant connections, the LFIx output can be used to select an alternate data stream. When an LFIx indication is detected, external logic can toggle selection of the associated INx1± and INx2± input through the associated INSELx input. When a port switch takes place, it is necessary for the receive PLL for that channel to reacquire the new serial stream and frame to the incoming character boundaries.

Deserializer/Framer

Each CDR circuit extracts bits from the associated serial data stream and clocks these bits into the Shifter/Framer at the bit-clock rate. When enabled, the Framer examines the data stream looking for one or more COMMA or K28.5 characters at all possible bit positions. The location of this character in the data stream is used to determine the character boundaries of all following characters.

Framing Character

The CYP15G0403DXB allows selection of different framing characters on each channel. Two combinations of framing characters are supported to meet the requirements of different interfaces. The selection of the framing character is made through the FRAMCHARx latches via the configuration interface.

The specific bit combinations of these framing characters are listed in Table 6. When the specific bit combination of the selected framing character is detected by the framer, the boundaries of the characters present in the received data stream are known.

Table 6. Framing Character Selector

FRAMCHARx	Bits detected in framer	
	Character Name	Bits Detected
0	COMMA+ COMMA–	00111110XX[8] or 11000001XX
1	–K28.5 +K28.5	0011111010 or 1100000101

Framer

The framer on each channel operates in one of three different modes. Each framer may be enabled or disabled using the RFENx latches via the configuration interface. When the framer is disabled (RFENx = 0), no combination of received bits alters the frame information.

When the Low-Latency framer is selected (RFMODEx[1:0] = 00), the framer operates by stretching the recovered character clock until it aligns with the received character boundaries. In this mode the framer starts its alignment process on the first detection of the selected framing character. To reduce the impact on external circuits that use the recovered clock, the clock period is not stretched by more than two bit-periods in any one clock cycle. When operated with a character-rate output clock, the output of properly framed characters may be delayed by up to nine character-clock cycles from the detection of the selected framing character. When operated with a half-character-rate output clock, the output of properly framed characters may be delayed by up to 14 character-clock cycles from the detection of the framing character.

Note. When Receive BIST is enabled on a channel, the Low-Latency Framer must not be enabled. The BIST sequence contains an aliased K28.5 framing character, which causes the Receiver to update its character boundaries incorrectly.

When RFMODEx[1:0] = 10, the Cypress-Mode Multi-Byte framer is selected. The required detection of multiple framing characters makes the associated link much more robust to incorrect framing due to aliased SYNC characters in the data stream. In this mode, the framer does not adjust the character clock boundary, but instead aligns the character to the already recovered character clock. This ensures that the recovered clock does not contain any significant phase changes or hops during normal operation or framing, and allows the recovered clock to be replicated and distributed to other external circuits or components using PLL-based clock distribution elements. In this framing mode the character boundaries are only adjusted if the selected framing character is detected at least twice within a span of 50 bits, with both instances on identical 10-bit character boundaries.

When RFMODEx[1:0] = 01, the Alternate-mode Multi-Byte Framer is enabled. Like the Cypress-mode Multi-Byte Framer, multiple framing characters must be detected before the character boundary is adjusted. In this mode, the data stream must contain a minimum of four of the selected framing characters, received as consecutive characters, on identical 10-bit boundaries, before character framing is adjusted.

10B/8B Decoder Block

The decoder logic block performs two primary functions:

- decoding the received transmission characters to Data and Special Character codes
- comparing generated BIST patterns with received characters to permit at-speed link and device testing.

The framed parallel output of each deserializer shifter is passed to its associated 10B/8B Decoder where, if the decoder is enabled, the input data is transformed from a 10-bit transmission character back to the original Data or Special Character code. This block uses the 10B/8B decoder patterns in Table 15 on page 42 and Table 16 on page 46. Received Special Code characters are decoded using Table 16. Valid data characters are indicated by a 000b bit-combination on the associated RXSTx[2:0] status bits, and Special Character codes are indicated by a 001b bit-combination of these status outputs. Framing characters, Invalid patterns, disparity errors, and synchronization status are presented as alternate combinations of these status bits.

When DECBYPx = 0, the 10B/8B decoder is bypassed via the configuration interface. When bypassed, raw 10-bit characters are passed through the receiver and presented at the RXDx[7:0] and the RXSTA[1:0] outputs as 10-bit wide characters.

When the decoder is enabled by setting DECBYPx = 1 via the configuration interface, the 10-bit transmission characters are decoded using Table 15 and Table 16. Received Special characters are decoded using Table 16. The columns used in Table 16 are determined by the DECMODEx latch via the device configuration interface. When DECMODEx = 0 the ALTERNATE table is used and when DECMODEx = 1 the CYPRESS table is used.

Receive BIST Operation

The receiver channel contains an internal pattern checker that can be used to validate both device and link operation. These pattern checkers are enabled by the associated RXBISTx latch via the device configuration interface. When enabled, a register

Note
7. The peak amplitudes listed in this table are for typical waveforms that have generally 3–4 transitions for every ten bits. In a worse case environment the signals may have a sine-wave appearance (highest transition density with repeating 0101...). Signal peak amplitudes levels within this environment type could increase the values in the table above by approximately 100 mV.

Note
8. The standard definition of a Comma contains only seven bits. However, since all valid Comma characters within the 8B/10B character set also have the eighth bit as an inversion of the seventh bit, the compare pattern is extended to a full eight bits to reduce the possibility of a framing error.

in the associated receive channel becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character or 526-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXSTx[2:0] bits of the Output Register.

When BIST is first recognized as being enabled in the Receiver, the LFSR is preset to the BIST-loop start-code of D0.0. This code D0.0 is sent only once per BIST loop. The status of the BIST progress and any character mismatches are presented on the RXSTx[2:0] status outputs.

Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXSTx[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the decoder is bypassed and BIST is enabled on a receive channel.

The specific status reported by the BIST state machine are listed in Table 11 on page 28. These same codes are reported on the receive status outputs.

The specific patterns checked by each receiver are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence compared by the CYP15G0403DXB is identical to that in the CY7B933, CY7C924DX, and CYP15G0401DXB, allowing interoperable systems to be built when used at compatible serial signaling rates.

If the number of invalid characters received ever exceeds the number of valid characters by 16, the receive BIST state machine aborts the compare operations and resets the LFSR to the D0.0 state to look for the start of the BIST sequence again.

When the receive paths are configured for REFCLKx± operation, each pass must be preceded by a 16-character Word Sync Sequence to allow management of clock frequency variations.

The receive BIST state machine requires the characters to be correctly framed for it to detect the BIST sequence. If the Low Latency Framer is enabled, the Framer misaligns to an aliased SYNC character within the BIST sequence. If the Alternate Multi-Byte Framer is enabled and the Receiver outputs are clocked relative to a recovered clock, it is generally necessary to frame the receiver before BIST is enabled. If the receive outputs are clocked relative to REFCLKx±, the transmitter precedes every 511 character BIST sequence with a 16 character-character Word Sync Sequence.

A device reset ($\overline{\text{RESET}}$ sampled LOW) presets the BIST Enable Latches to disable BIST on all channels.

Receive Elasticity Buffer

Each receive channel contains an Elasticity Buffer that is designed to support multiple clocking modes. These buffers allow data to be read using a clock that is asynchronous in both frequency and phase from the Elasticity Buffer write clock, or to be read using a clock that is frequency coherent but with uncontrolled phase relative to the Elasticity Buffer write clock.

If the chip is configured for operation with a recovered clock, the Elasticity Buffer is bypassed.

Each Elasticity Buffer is 10 characters deep, and supports and an 11 bit wide data path. It is capable of supporting a decoded character and three status bits for each character present in the buffer. The write clock for these buffers is always the recovered clock for the associated read channel.

Receive Modes

When the receive channel is clocked by REFCLKx±, the RXCLKx± outputs present a buffered or divided (depending on RXRATEx) and delayed form of REFCLKx±. In this mode, the receive Elasticity Buffers are enabled. For REFCLKx± clocking, the Elasticity Buffers must be able to insert K28.5 characters and delete framing characters as appropriate.

The insertion of a K28.5 or deletion of a framing character can occur at any time on any channel, however, the actual timing of these insertions and deletions is controlled in part by how the transmitter sends its data. Insertion of a K28.5 character can only occur when the receiver has a framing character in the Elasticity Buffer. Likewise, to delete a framing character, one must also be in the Elasticity Buffer. To prevent a buffer overflow or underflow on a receive channel, a minimum density of framing characters must be present in the received data streams.

When the receive channel Output Register is clocked by a recovered clock, no characters are added or deleted and the receiver Elasticity Buffer is bypassed.

Power Control

The CYP15G0403DXB supports user control of the powered up or down state of each transmit and receive channel. The receive channels are controlled by the RXPLLPDx latch via the device configuration interface. When RXPLLPDx = 0, the associated PLL and analog circuitry of the channel is disabled. The transmit channels are controlled by the OE1x and the OE2x latches via the device configuration interface. When a driver is disabled via the configuration interface, it is internally powered down to reduce device power. If both serial drivers for a channel are in this disabled state, the associated internal logic for that channel is also powered down.

Device Reset State

When the CYP15G0403DXB is reset by assertion of $\overline{\text{RESET}}$, all state machines, counters, and configuration latches in the device are initialized to a reset state, and the Elasticity Buffer pointers are set to a nominal offset. Additionally, the JTAG controller must also be reset to ensure valid operation (even if JTAG testing is not performed). See "JTAG Support" on page 27 for JTAG state machine initialization. See Table 9 on page 22 for the initialize values of the configuration latches.

Following a device reset, it is necessary to enable the transmit and receive channels used for normal operation. This can be done by sequencing the appropriate values on the device configuration interface.[4]

CYP15G0403DXB

Output Bus

Each receive channel presents an 11-signal output bus consisting of

- an 8-bit data bus
- a 3-bit status bus.

The signals present on this output bus are modified by the present operating mode of the CYP15G0403DXB as selected by the DECBYPx configuration latch. This mapping is shown in Table 7.

Table 7. Output Register Bit Assignments

Signal Name	BYPASS ACTIVE (DECBYPx = 0)	DECODER (DECBYP = 1)
RXSTx[2] (LSB)	COMDETx	RXSTx[2]
RXSTx[1]	DOUTx[0]	RXSTx[1]
RXSTx[0]	DOUTx[1]	RXSTx[0]
RXDx[0]	DOUTx[2]	RXDx[0]
RXDx[1]	DOUTx[3]	RXDx[1]
RXDx[2]	DOUTx[4]	RXDx[2]
RXDx[3]	DOUTx[5]	RXDx[3]
RXDx[4]	DOUTx[6]	RXDx[4]
RXDx[5]	DOUTx[7]	RXDx[5]
RXDx[6]	DOUTx[8]	RXDx[6]
RXDx[7] (MSB)	DOUTx[9]	RXDx[7]

When the 10B/8B decoder is bypassed, the framed 10-bit value is presented to the associated Output Register, along with a status output signal indicating if the character in the Output Register is one of the selected framing characters. The bit usage and mapping of the external signals to the raw 10B transmission character is shown in Table 8.

Table 8. Decoder Bypass Mode

Signal Name	Bus Weight	10 Bit Name
RXSTx[2] (LSB)	COMDETx	
RXSTx[1]	2^0	a
RXSTx[0]	2^1	b
RXDx[0]	2^2	c
RXDx[1]	2^3	d
RXDx[2]	2^4	e
RXDx[3]	2^5	i
RXDx[4]	2^6	f
RXDx[5]	2^7	g
RXDx[6]	2^8	h
RXDx[7] (MSB)	2^9	j

The COMDETx status output operates the same regardless of the bit combination selected for character framing by the FRAMCHARx latch. COMDETx is HIGH when the character in the output register contains the selected framing character at the proper character boundary, and LOW for all other bit combinations.

When the low-latency framer and half-rate receive port clocking are also enabled, the framer stretches the recovered clock to the nearest 20-bit boundary such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

When the Cypress or Alternate Mode Framer is enabled and half-rate receive port clocking is also enabled, the output clock is not modified when framing is detected, but a single pipeline stage may be added or subtracted from the data stream by the framer logic such that the rising edge of RXCLKx+ occurs when COMDETx is present on the associated output bus.

This adjustment only occurs when the framer is enabled. When the framer is disabled, the clock boundaries are not adjusted, and COMDETx may be asserted during the rising edge of RXCLKx– (if an odd number of characters were received following the initial framing).

Receive Status Bits

When the 10B/8B decoder is enabled, each character presented at the Output Register includes three associated status bits. These bits are used to identify

- if the contents of the data bus are valid,
- the type of character present,
- the state of receive BIST operations,
- character violations.

These conditions often overlap; e.g. a valid data character received with incorrect running disparity is not reported as a valid data character. It is instead reported as a decoder violation of some specific type. This implies a hierarchy or priority level to the various status bit combinations. The hierarchy and value of each status are listed in Table 11.

A second status mapping, listed in Table 11, is used when the receive channel is configured for BIST operation. This status is used to report receive BIST status and progress.

BIST Status State Machine

When a receive path is enabled to look for and compare the received data stream with the BIST pattern, the RXSTx[2:0] bits identify the present state of the BIST compare operation.

The BIST state machine has multiple states, as shown in Figure 2 and Table 11. When the receive PLL detects an out-of-lock condition, the BIST state is forced to the Start-of-BIST state, regardless of the present state of the BIST state machine. If the number of detected errors ever exceeds the number of valid matches by greater than 16, the state machine is forced to the WAIT_FOR_BIST state where it monitors the receive path for the first character of the next BIST sequence (D0.0). Also, if the Elasticity Buffer ever hits an overflow/underflow condition, the status is forced to the BIST_START until the buffer is re-centered (approximately nine character periods).

To ensure compatibility between the source and destination systems when operating in BIST modes, the sending and receiving ends of the link must use the same receive clock configuration.

in the associated receive channel becomes a signature pattern generator and checker by logically converting to a Linear Feedback Shift Register (LFSR). This LFSR generates a 511-character or 526-character sequence that includes all Data and Special Character codes, including the explicit violation symbols. This provides a predictable yet pseudo-random sequence that can be matched to an identical LFSR in the attached Transmitter(s). When synchronized with the received data stream, the associated Receiver checks each character in the Decoder with each character generated by the LFSR and indicates compare errors and BIST status at the RXSTx[2:0] bits of the Output Register.

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Code rule violations or running disparity errors that occur as part of the BIST loop do not cause an error indication. RXSTx[2:0] indicates 010b or 100b for one character period per BIST loop to indicate loop completion. This status can be used to check test pattern progress. These same status values are presented when the decoder is bypassed and BIST is enabled on a receive channel.

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The specific patterns checked by each receiver are described in detail in the Cypress application note "HOTLink Built-In Self-Test." The sequence compared by the CYP15G0403DXB is identical to that in the CY7B933, CY7C924DX, and CYP15G0401DXB, allowing interoperable systems to be built when used at compatible serial signaling rates.

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This adjustment only occurs when the framer is enabled. When the framer is disabled, the clock boundaries are not adjusted, and COMDETx may be asserted during the rising edge of RXCLKx– (if an odd number of characters were received following the initial framing).

Receive Status Bits

When the 10B/8B decoder is enabled, each character presented at the Output Register includes three associated status bits. These bits are used to identify

- if the contents of the data bus are valid,
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To ensure compatibility between the source and destination systems when operating in BIST modes, the sending and receiving ends of the link must use the same receive clock configuration.