ANALOG DEVICES

1 GHz, 5,500 V/μs Low Distortion Amplifier

AD8009

FEATURES

Ultrahigh Speed
- 5,500 V/μs Slew Rate, 4 V Step, G = +2
- 545 ps Rise Time, 2 V Step, G = +2
- Large Signal Bandwidth
  - 440 MHz, G = +2
  - 320 MHz, G = +10
- Small Signal Bandwidth (–3 dB)
  - 1 GHz, G = +1
  - 700 MHz, G = +2
- Settling Time 10 ns to 0.1%, 2 V Step, G = +2

Low Distortion Over Wide Bandwidth
- SFDR
  - –44 dBc @ 150 MHz, G = +2, V_O = 2 V p-p
  - –41 dBc @ 150 MHz, G = +10, V_O = 2 V p-p
- 3rd Order Intercept (3IP)
  - 26 dBm @ 70 MHz, G = +10
  - 18 dBm @ 150 MHz, G = +10

Good Video Specifications
- Gain Flatness 0.1 dB to 75 MHz
- 0.01% Differential Gain Error, R_L = 150 Ω
- 0.01° Differential Phase Error, R_L = 150 Ω

High Output Drive
- 175 mA Output Load Drive
- 10 dBm with –38 dBc SFDR @ 70 MHz, G = +10

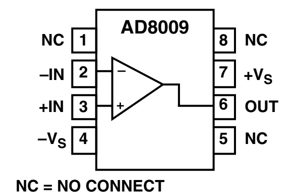
Supply Operation
- ±5 V Voltage Supply
- 14 mA (Typ) Supply Current

APPLICATIONS

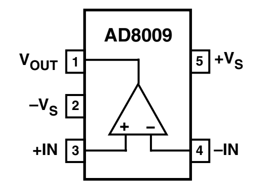
- Pulse Amplifier
- IF/RF Gain Stage/Amplifiers
- High Resolution Video Graphics
- High Speed Instrumentations
- CCD Imaging Amplifier

FUNCTIONAL BLOCK DIAGRAMS

8-Lead Plastic SOIC (SO-8)



5-Lead SOT-23 (RT-5)



PRODUCT DESCRIPTION

The AD8009 is an ultrahigh speed current feedback amplifier with a phenomenal 5,500 V/μs slew rate that results in a rise time of 545 ps, making it ideal as a pulse amplifier.

The high slew rate reduces the effect of slew rate limiting and results in the large signal bandwidth of 440 MHz required for high resolution video graphic systems. Signal quality is maintained over a wide bandwidth with worst case distortion of –40 dBc @ 250 MHz (G = +10, 1 V p-p). For applications with multitone signals such as IF signal chains, the third order Intercept (3IP) of 12 dBm is achieved at the same frequency. This distortion performance coupled with the current feedback architecture make the AD8009 a flexible component for a gain stage amplifier in IF/RF signal chains.

The AD8009 is capable of delivering over 175 mA of load current and will drive four back terminated video loads while maintaining low differential gain and phase error of 0.02% and 0.04° respectively. The high drive capability is also reflected in the ability to deliver 10 dBm of output power @ 70 MHz with –38 dBc SFDR.

The AD8009 is available in a small SOIC package and will operate over the industrial temperature range –40°C to +85°C. The AD8009 is also available in an SOT-23-5 and will operate over the commercial temperature range 0°C to +70°C.

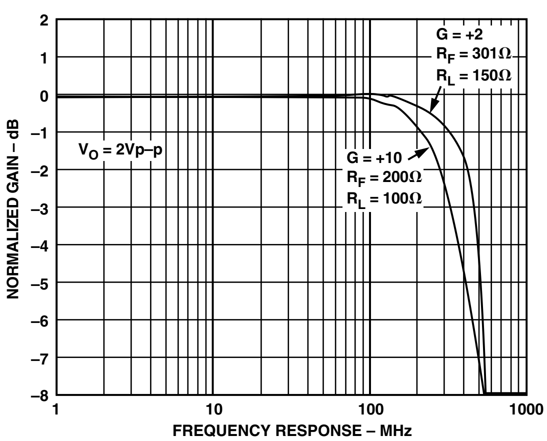


Figure 1. Large Signal Frequency Response; G = +2 & +10

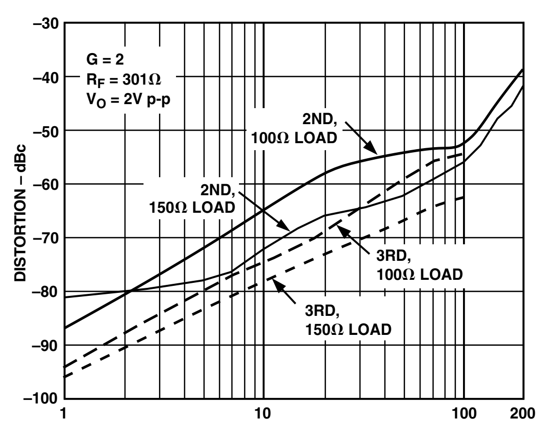


Figure 2. Distortion vs. Frequency; G = +2

REV. C

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AD8009–SPECIFICATIONS

(@ T_A = 25°C, V_S = ±5 V, R_L = 100 Ω, for R Package: R_F = 301 Ω for G = +1, +2, R_F = 200 Ω for G = +10, for RT Package: R_F = 332 Ω for G = +1, R_F = 226 Ω for G = +2 and R_F = 191 for G = +10, unless otherwise noted.)

Model	Conditions	AD8009AR/JRT Min	Typ	Max	Units
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth, V_O = 0.2 V p-p					
R Package	G = +1, R_F = 301 Ω		1000		MHz
RT Package	G = +1, R_F = 332 Ω		845		MHz
	G = +2	480	700		MHz
	G = +10	300	350		MHz
Large Signal Bandwidth, V_O = 2 V p-p	G = +2	390	440		MHz
	G = +10	235	320		MHz
Gain Flatness 0.1 dB, V_O = 0.2 V p-p	G = +2, R_L = 150 Ω	45	75		MHz
Slew Rate	G = +2, R_L = 150 Ω, 4 V Step	4500	5500		V/µs
Settling Time to 0.1%	G = +2, R_L = 150 Ω, 2 V Step		10		ns
	G = +10, 2 V Step		25		ns
Rise and Fall Time	G = +2, R_L = 150 Ω, 4 V Step		0.725		ns
HARMONIC/NOISE PERFORMANCE					
SFDR G = +2, V_O = 2 V p-p	5 MHz		–74		dBc
	70 MHz		–53		dBc
	150 MHz		–44		dBc
G = +10, V_O = 2 V p-p	5 MHz		–58		dBc
	70 MHz		–41		dBc
	150 MHz		–41		dBc
Third Order Intercept (3IP)	70 MHz		26		dBm
W.R.T. Output, G = +10	150 MHz		18		dBm
	250 MHz		12		dBm
Input Voltage Noise	f = 10 MHz		1.9		nV/√Hz
Input Current Noise	f = 10 MHz, +In		46		pA/√Hz
	–In		41		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.01	0.03	%
	R_L = 37.5 Ω		0.02	0.05	%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.01	0.03	Degrees
	R_L = 37.5 Ω		0.04	0.08	Degrees
DC PERFORMANCE					
Input Offset Voltage			2	5	mV
	T_{MIN}–T_{MAX}			7	mV
Offset Voltage Drift			4		µV/°C
–Input Bias Current			50	150	±µA
	T_{MIN}–T_{MAX}		75		±µA
+Input Bias Voltage			50	150	±µA
	T_{MIN}–T_{MAX}		75		±µA
Open Loop Transresistance		90	250		kΩ
	T_{MIN}–T_{MAX}		170		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		110		kΩ
	–Input		8		Ω
Input Capacitance	+Input		2.6		pF
Input Common-Mode Voltage Range			3.8		±V
Common-Mode Rejection Ratio	V_{CM} = ±2.5	50	52		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		±3.7	±3.8		V
Output Current	R_L = 10 Ω, P_D Package = 0.7 W	150	175		mA
Short Circuit Current			330		mA
POWER SUPPLY					
Operating Range		±4		±6	V
Quiescent Current			14	16	mA
	T_{MIN}–T_{MAX}			18	mA
Power Supply Rejection Ratio	V_S = ±4 V to ±6 V	64	70		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . 12.6 V
Internal Power Dissipation[2]
Small Outline Package (R) . . . . 0.75 Watts
Input Voltage (Common Mode) . . . . $\pm V_S$
Differential Input Voltage . . . . ±3.5 V
Output Short Circuit Duration
. . . . Observe Power Derating Curves
Storage Temperature Range R Package . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Operating Temperature Range (J Grade) . . . . . . 0°C to +70°C
Lead Temperature Range (Soldering 10 sec) . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead SOIC Package: θ_{JA} = 155°C/W.
5-Lead SOT-23 Package: θ_{JA} = 240°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8009 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure.

While the AD8009 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves.

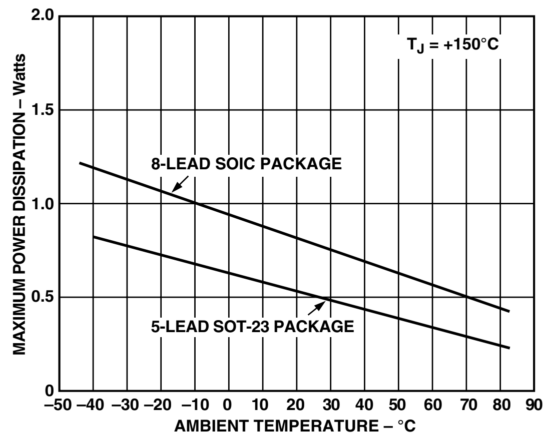


Figure 3. Plot of Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
AD8009ACHIPS	–40°C to +85°C	Die		
AD8009AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8009AR-REEL	–40°C to +85°C	8-Lead SOIC	13" Tape and Reel	
AD8009AR-REEL7	–40°C to +85°C	8-Lead SOIC	7" Tape and Reel	
AD8009JRT-REEL	0°C to +70°C	5-Lead SOT-23	13" Tape and Reel	HKJ
AD8009JRT-REEL7	0°C to +70°C	5-Lead SOT-23	7" Tape and Reel	HKJ
AD8009-EB		Evaluation Board	SO-8	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8009 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

AD8009–Typical Performance Characteristics

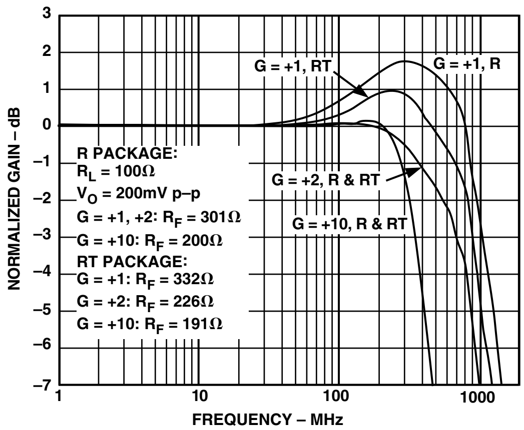


Figure 4. Frequency Response; G = +1, +2, +10, R and RT Packages

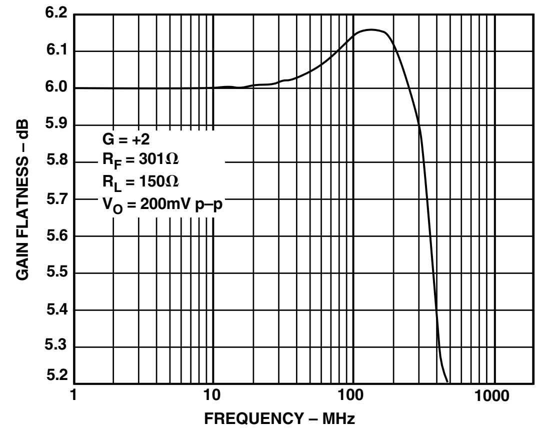


Figure 7. Gain Flatness; G = +2

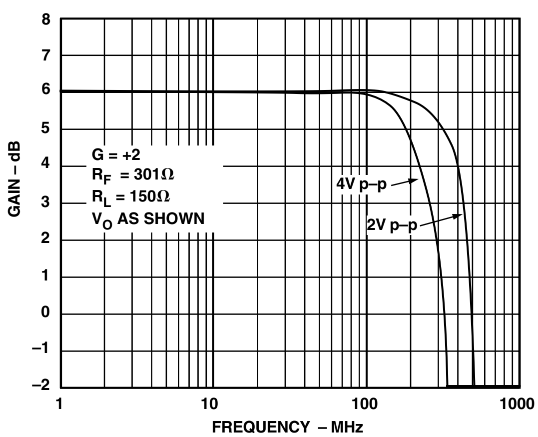


Figure 5. Large Signal Frequency Response; G = +2

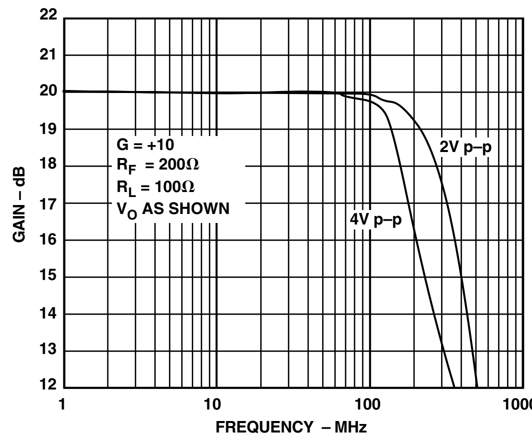


Figure 8. Large Signal Frequency Response; G = +10

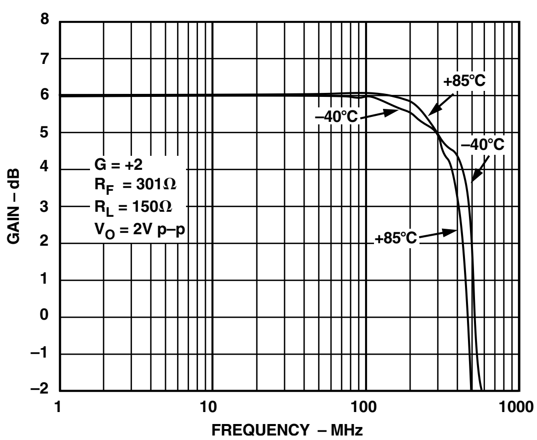


Figure 6. Large Signal Frequency Response vs. Temperature; G = +2

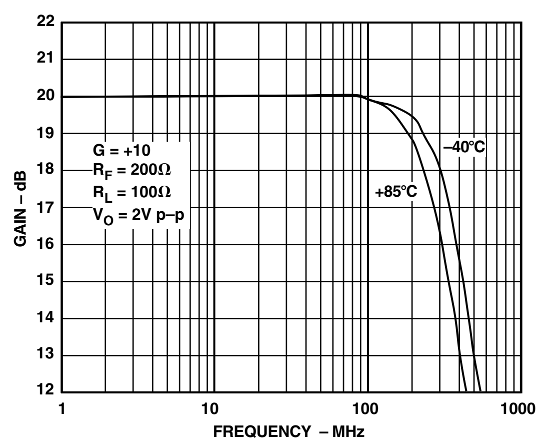


Figure 9. Large Signal Frequency Response vs. Temperature; G = +10

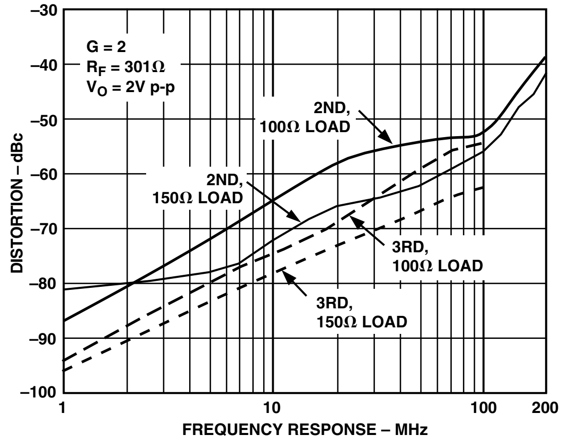


Figure 10. Distortion vs. Frequency; G = +2

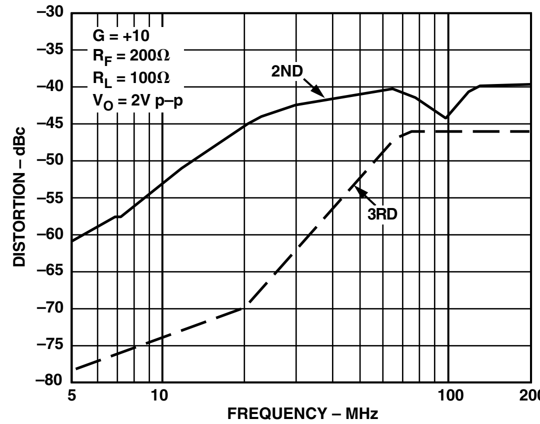


Figure 13. Distortion vs. Frequency; G = +10

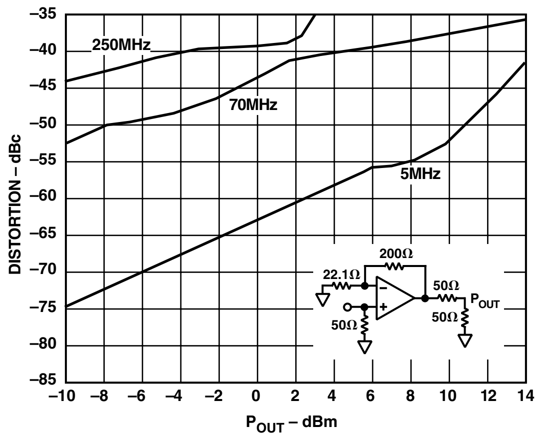


Figure 11. 2nd Harmonic Distortion vs. P_{OUT}; (G = +10)

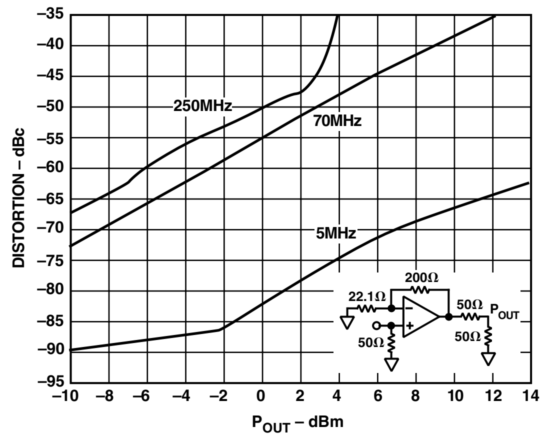


Figure 14. 3rd Harmonic Distortion vs. P_{OUT}; (G = +10)

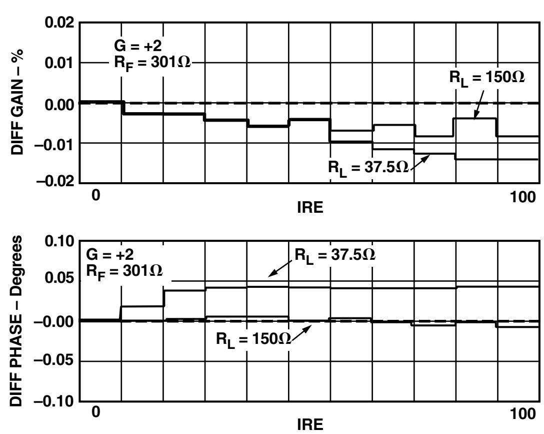


Figure 12. Differential Gain and Phase

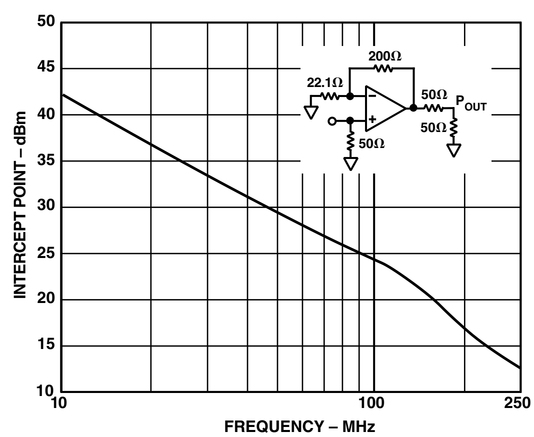


Figure 15. Two Tone, 3rd Order IMD Intercept vs. Frequency; G = +10

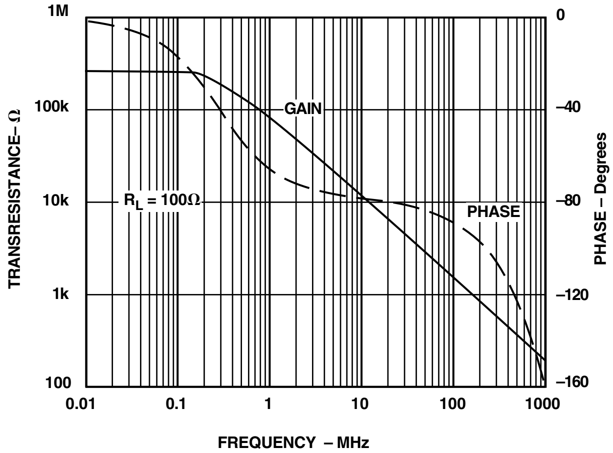


Figure 16. Transresistance and Phase vs. Frequency

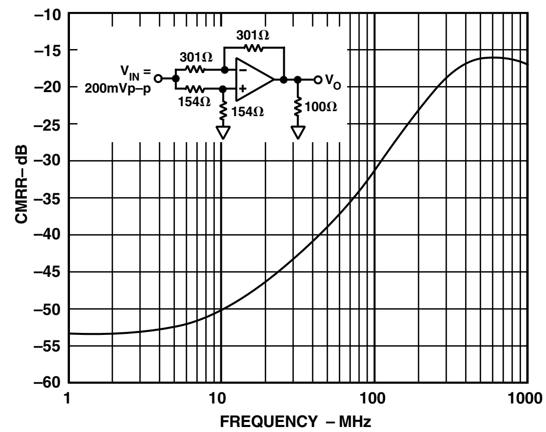


Figure 19. CMRR vs. Frequency

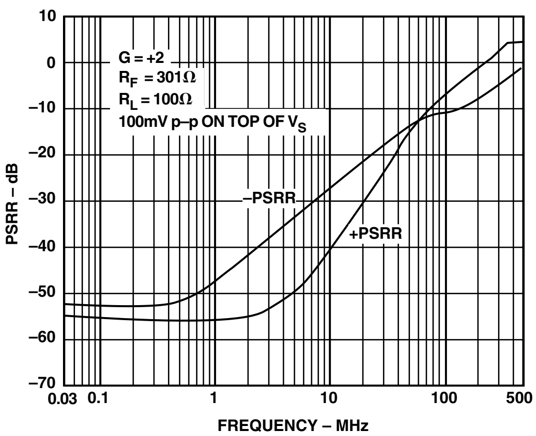


Figure 17. PSRR vs. Frequency

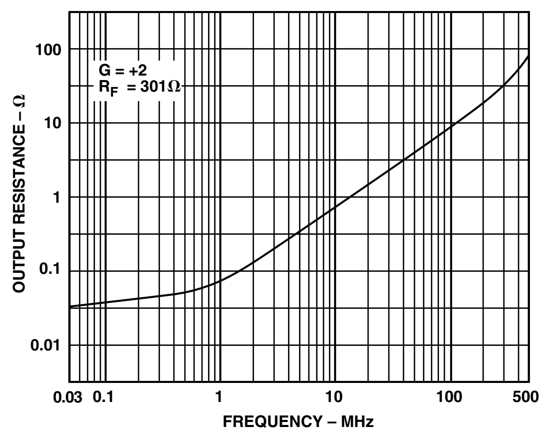


Figure 20. Output Resistance vs. Frequency

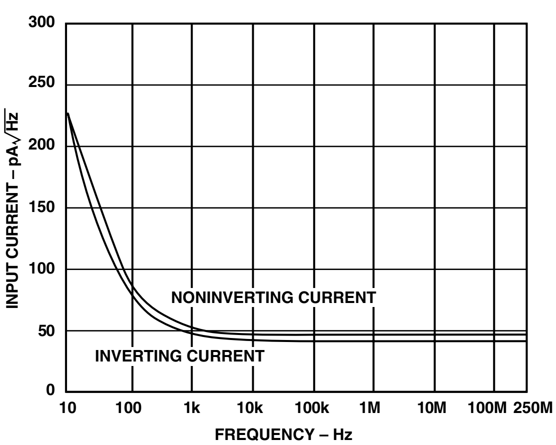


Figure 18. Current Noise vs. Frequency

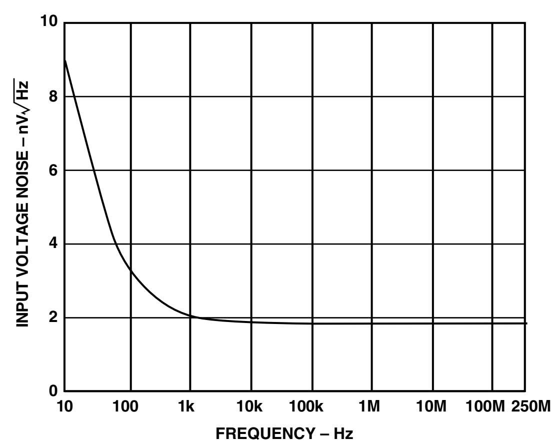


Figure 21. Voltage Noise vs. Frequency

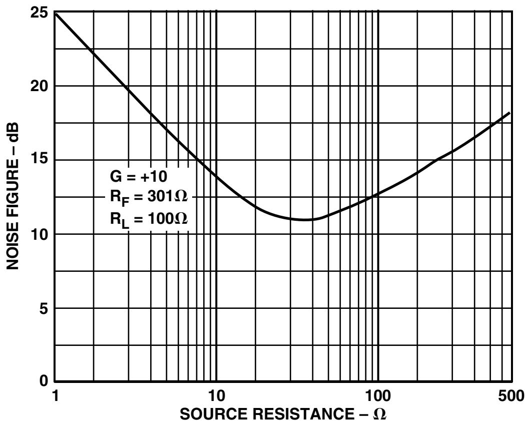


Figure 22. Noise Figure

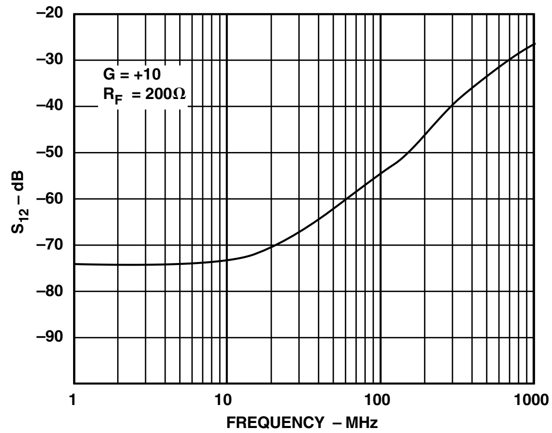


Figure 25. Reverse Isolation (S_{12}); G = +10

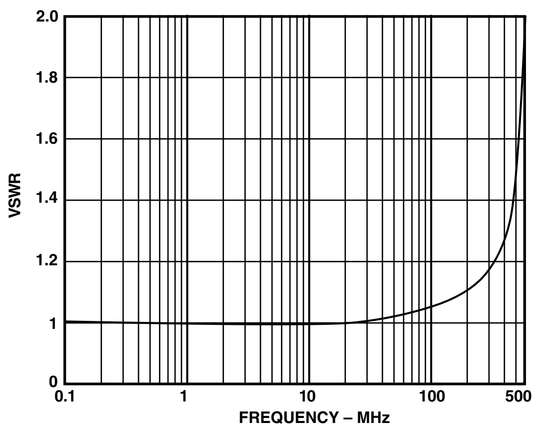


Figure 23. Input VSWR; G = +10

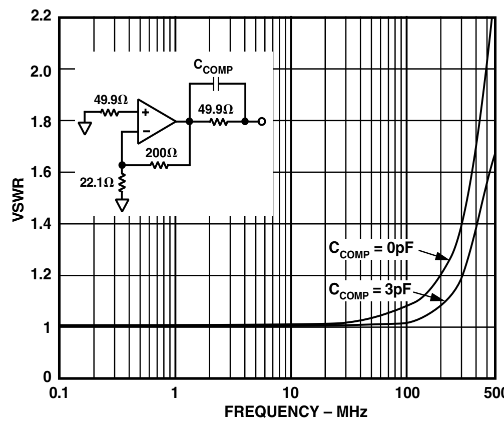


Figure 26. Output VSWR; G = +10

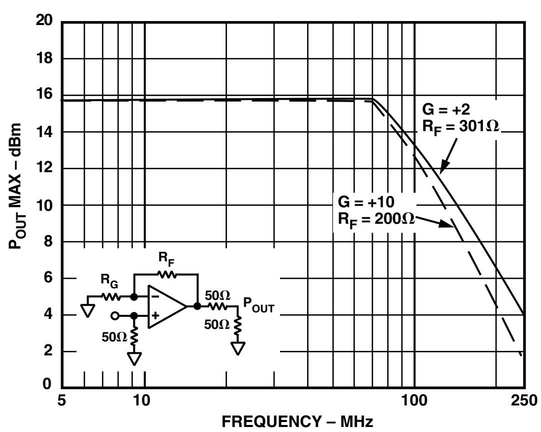


Figure 24. Maximum Output Power vs. Frequency

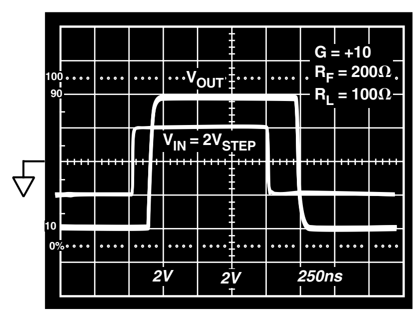


Figure 27. Overdrive Recovery; G = +10

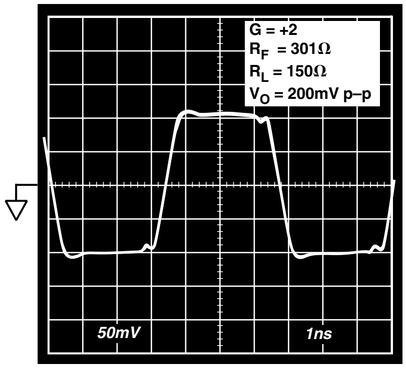


Figure 28. Small Signal Transient Response; G = +2

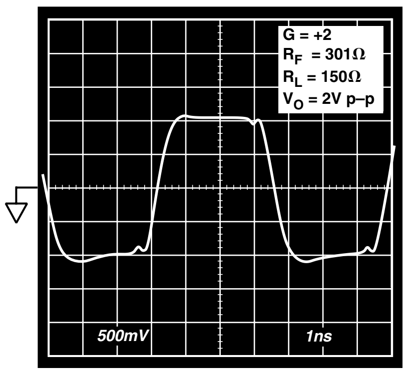


Figure 29. 2 V Transient Response; G = +2

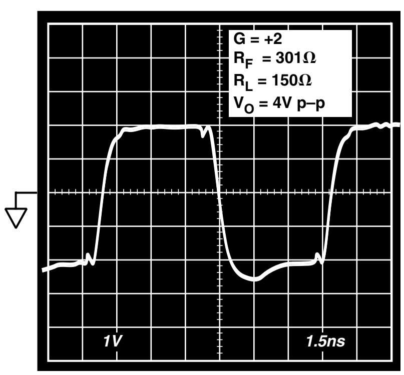


Figure 30. 4 V Transient Response; G = +2

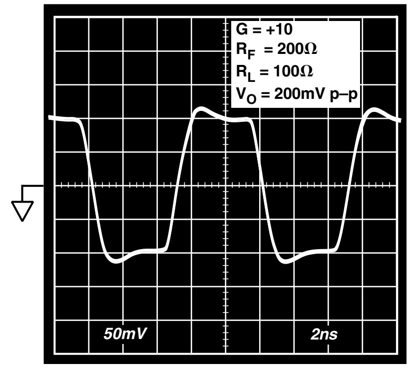


Figure 31. Small Signal Transient Response; G = +10

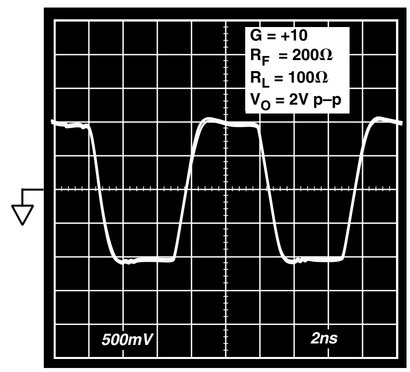


Figure 32. 2 V Transient Response; G = +10

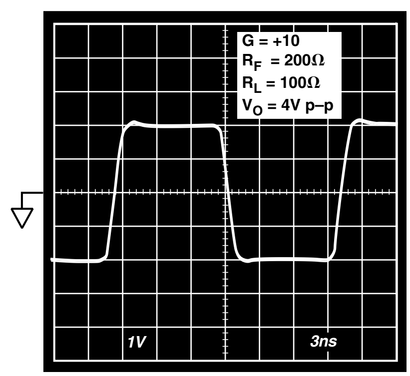


Figure 33. 4 V Transient Response; G = +10

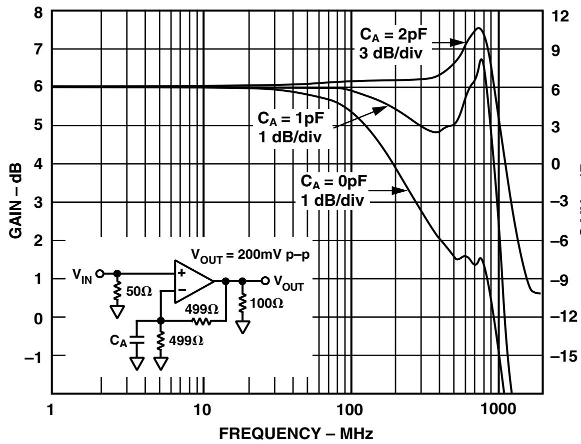


Figure 34. Small Signal Frequency Response vs. Parasitic Capacitance

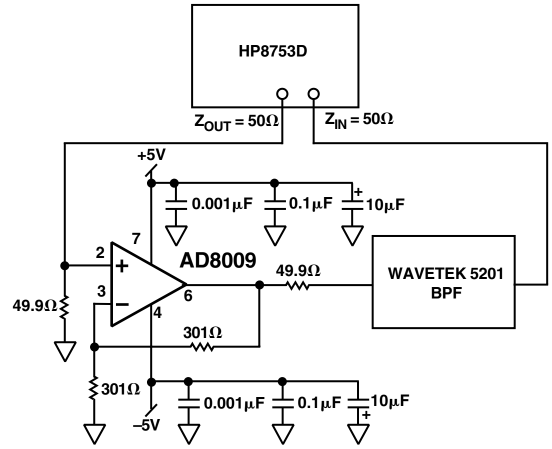


Figure 36. AD8009 Driving a Bandpass RF Filter

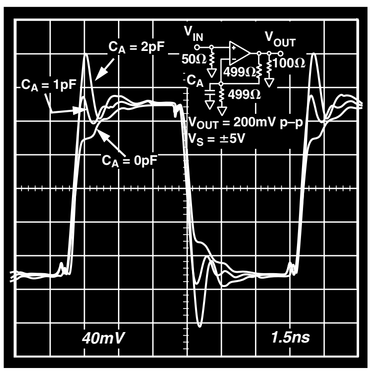


Figure 35. Small Signal Pulse Response vs. Parasitic Capacitance

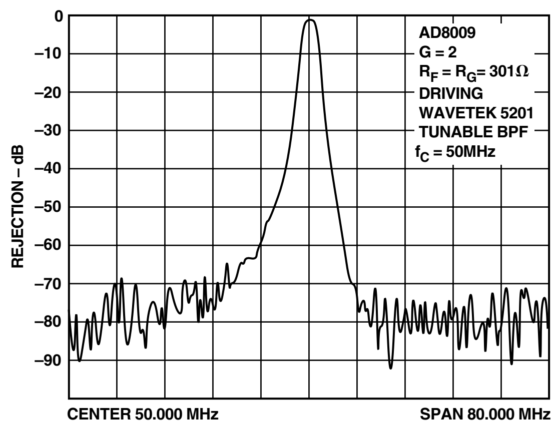


Figure 37. Frequency Response of Bandpass Filter Circuit

APPLICATIONS

All current feedback op amps are affected by stray capacitance on their –INPUT. Figures 34 and 35 illustrate the AD8009's response to such capacitance.

Figure 34 shows the bandwidth can be extended by placing a capacitor in parallel with the gain resistor. The small signal pulse response corresponding to such an increase in capacitance/ bandwidth is shown in Figure 35.

As a practical consideration, the higher the capacitance on the –INPUT to GND, the higher R_F needs to be to minimize peaking/ringing.

RF Filter Driver

The output drive capability, wide bandwidth and low distortion of the AD8009 are well suited for creating gain blocks that can drive RF filters. Many of these filters require that the input be driven by a 50 Ω source, while the output must be terminated in 50 Ω for the filters to exhibit their specified frequency response.

Figure 36 shows a circuit for driving and measuring the frequency response of a filter, a Wavetek 5201 Tunable Band Pass Filter that is tuned to a 50 MHz center frequency. The HP8753D network provides a stimulus signal for the measurement. The analyzer has a 50 Ω source impedance that drives a cable that is terminated in 50 Ω at the high impedance noninverting input of the AD8009.

The AD8009 is set at a gain of two. The series 50 Ω resistor at the output, along with the 50 Ω termination provided by the filter and its termination, yield an overall unity gain for the measured path. The frequency response plot of Figure 37 shows the circuit to have an insertion loss of 1.3 dB in the pass band and about 75 dB rejection in the stop band.

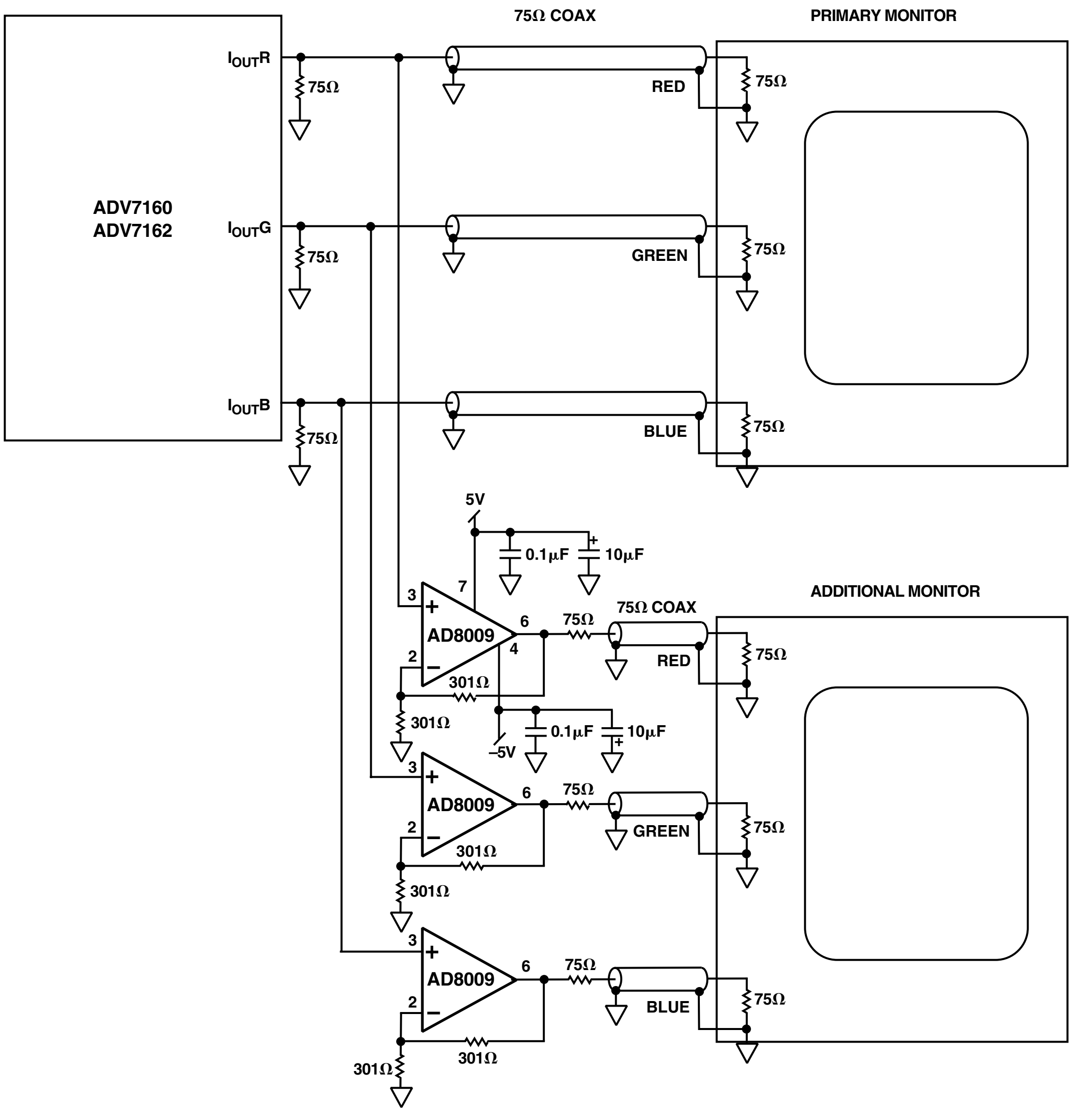


Figure 38. Driving an Additional High Resolution Monitor Using Three AD8009s

RGB Monitor Driver

High resolution computer monitors require very high full power bandwidth signals to maximize their display resolution. The RGB signals that drive these monitors are generally provided by a current-out RAMDAC that can directly drive a 75 Ω doubly terminated line.

There are times when the same output wants to be delivered to additional monitors. The termination provided internally by each monitor prohibits the ability to simply connect a second monitor in parallel with the first. Additional buffering must be provided.

Figure 38 shows a connection diagram for two high resolution monitors being driven by an ADV7160 or ADV7162, a 220 MHz (Mega-pixel per second) triple RAMDAC. This pixel rate requires a driver whose full power bandwidth is at least half the pixel rate or 110 MHz. This is to provide good resolution for a worst case signal that swings between zero scale and full scale on adjacent pixels.

The primary monitor is connected in the conventional fashion with a 75 Ω termination to ground at each end of the 75 Ω cable. Sometimes this configuration is called "doubly terminated" and is used when the driver is a high output impedance current source.

For the additional monitor, each of the RGB signals close to the RAMDAC output is applied to a high input impedance, noninverting input of an AD8009 that is configured for a gain of +2. The outputs each drive a series 75 Ω resistor, cable and termination resistor in the monitor that divides the output signal by two, thus providing an overall unity gain. This scheme is referred to as "back termination" and is used when the driver is a low output impedance voltage source. Back termination requires that the voltage of the signal be double the value that the monitor sees. Double termination requires that the output current be double the value that flows in the monitor termination.

Driving a Capacitive Load

A capacitive load, like that presented by some A/D converters, can sometimes be a challenge for an op amp to drive depending on the architecture of the op amp. Most of the problem is caused by the pole created by the output impedance of the op amp and the capacitor that is driven. This creates extra phase shift that can eventually cause the op amp to become unstable.

One way to prevent instability and improve settling time when driving a capacitor is to insert a resistor in series between the op amp output and the capacitor. The feedback resistor is still connected directly to the output of the op amp, while the series resistor provides some isolation of the capacitive load from the op amp output.

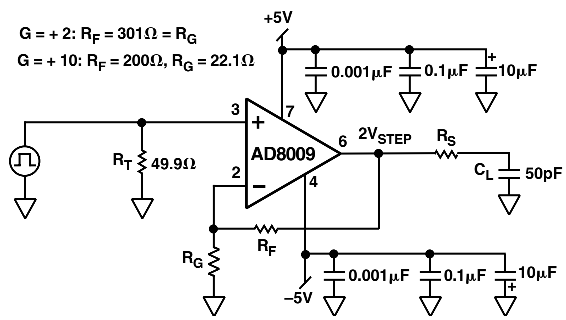


Figure 39. Capacitive Load Drive Circuit

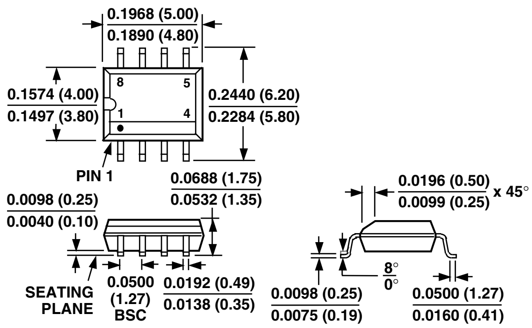
Figure 39 shows such a circuit with an AD8009 driving a 50 pF load. With R_S = 0, the AD8009 circuit will be unstable. For a gain of +2 and +10, it was found experimentally that setting R_S to 42.2 Ω will minimize the 0.1% settling time with a 2 V step at the output. The 0.1% settling time was measured to be 40 ns with this circuit.

For smaller capacitive loads, a smaller R_S will yield optimal settling time, while a larger R_S will be required for larger capacitive loads. Of course, a larger capacitance will always require more time for settling to a given accuracy than a smaller one, and this will be lengthened by the increase in R_S required. At best, a given RC combination will require about 7 time constants by itself to settle to 0.1%, so a limit will be reached where too large a capacitance cannot be driven by a given op amp and still meet the system's required settling time specification.

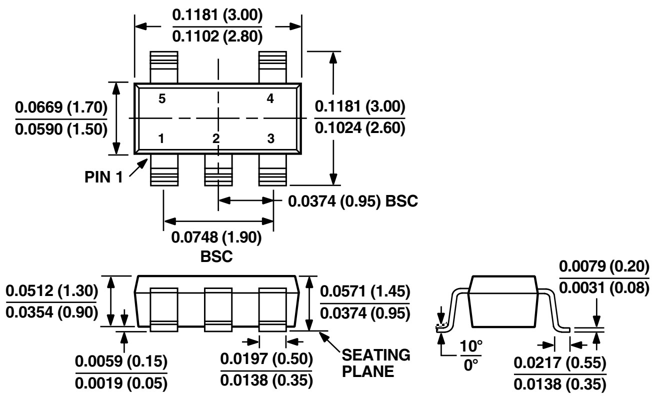
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (SO-8)



5-Lead Plastic Surface Mount (SOT-23) (RT-5)



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