MIC3003

FOM Management IC with Internal Calibration

General Description

The MIC3003 is a fiber optic module controller which enables the implementation of sophisticated, hot-pluggable fiber optic transceivers with intelligent laser control and an internally calibrated Digital Diagnostic Monitoring Interface per SFF-8472. It essentially integrates all non-datapath functions of an SFP transceiver into a tiny (4mm x 4mm) MLF® package. It also works well as a microcontroller peripheral in transponders or 10Gbps transceivers.

A highly configurable automatic power control (APC) circuit controls laser bias. Bias and modulation are temperature compensated using dual DACs, an on-chip temperature sensor, and NVRAM look-up tables. A programmable internal feedback resistor provides a wide dynamic range for the APC. Controlled laser turn-on facilitates hot plugging.

An analog-to-digital converter converts the measured temperature, voltage, bias current, transmit power, and received power from analog to digital. An EEPOT provides front-end adjustment of RX power. Each parameter is compared against user-programmed warning and alarm thresholds. Analog comparators and DACs provide fast monitoring of received power and critical laser operating parameters. Data can be reported as either internally calibrated or externally calibrated.

An interrupt output, power-on hour meter, and data-ready bits add user friendliness beyond SFF-8472. The interrupt output and data-ready bits reduce overhead in the host system. The power-on hour meter logs operating hours using an internal real-time clock and stores the result in NVRAM.

In addition to the features listed above which are already implemented in the previous MIC300x controllers, the MIC3003 features an extended temperature range, options to mask alarms and warnings interrupt and TXFAULT, a reset signal source, and the ability to support up to four chips with the same address on the serial interface. It also supports eight-byte SMBus block writes.

Communication with the MIC3003 is via an industry standard 2-wire SMBus serial interface. Nonvolatile memory is provided for serial ID, configuration, and separate OEM and user scratchpad spaces.

Datasheets and support documentation can be found on Micrel's web site at: www.micrel.com.

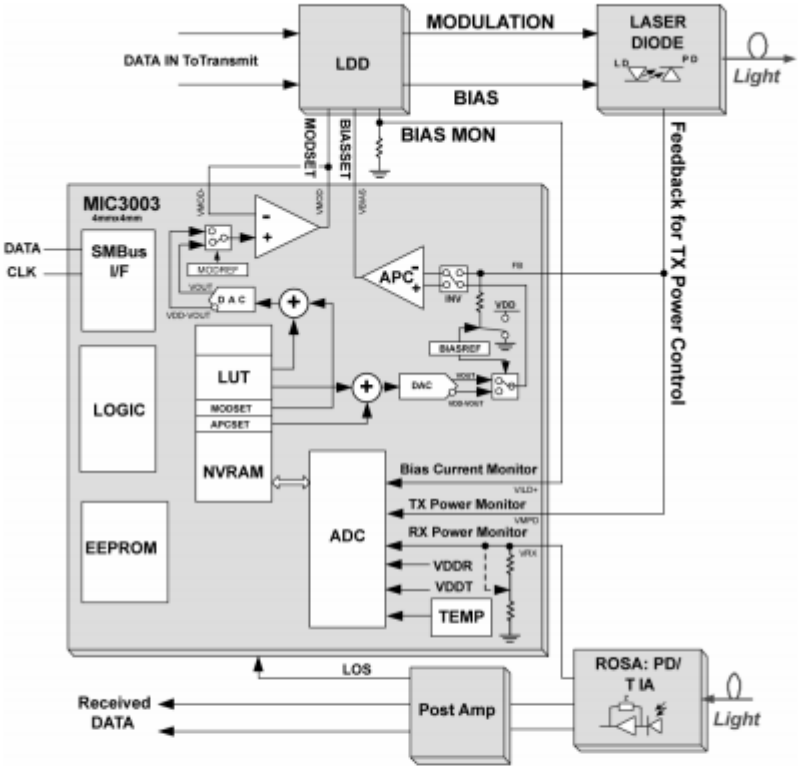
Features

- Extended temperature range
- Alarms and warnings interrupt and TXFAULT masks
- Capability to support up to four MIC3003 on one SMBus
- APC or constant-current laser bias
- Turbo mode for APC loop start-up and shorter laser turn on time
- Supports multiple laser types and bias circuit topologies
- Integrated digital temperature sensor
- Temperature compensation of modulation, bias, bias fault and alarm thresholds via NVRAM look-up tables
- NVRAM to support GBIC/SFP serial ID function
- User writable EEPROM scratchpad
- Reset signal compatible with some new systems requirements
- Diagnostic monitoring interface per SFF-8472
  - Monitors and reports critical parameters: temperature, bias current, TX and RX optical power, and supply voltage
  - S/W control and monitoring of TXFAULT, RXLOS, RATESELECT, and TXDISABLE
  - Internal or external calibration
  - EEPOT for adjusting RX power measurement
- Power-on hour meter
- Interrupt capability
- Extensive test and calibration features
- 2-wire SMBus-compatible serial interface
- SFP/SFP+ MSA and SFF-8472 compliant
- 3.0V to 3.6V power supply range
- 5V-tolerant I/O
- Available in (4mm x 4mm) 24-pin MLF® package

Applications

- SFP/SFP+ optical transceivers
- SONET/SDH transceivers and transponders
- Fibre Channel transceivers
- 10Gbps transceivers
- Free space optical communications
- Proprietary optical links

Typical Application



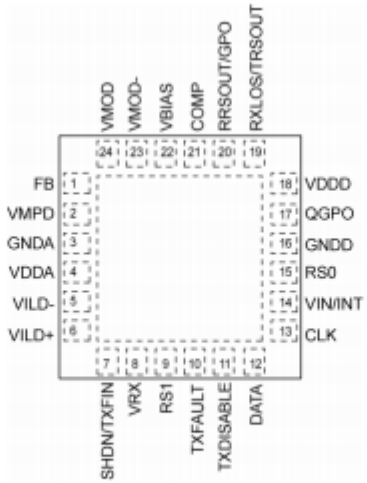
Ordering Information

Part Number	Package Type	Junction Temp. Range	Package Marking	Lead Finish
MIC3003GML	24-pin MLF®	–45°C to +105°C	3003 with Pb-Free bar-line indicator	Pb-Free NiPdAu
MIC3003GMLTR(1)	24-pin MLF®	–45°C to +105°C	3003 with Pb-Free bar-line indicator	Pb-Free NiPdAu

Note:

1. Tape and Reel.

Pin Configuration



24-Pin MLF® (MLF-24)

Pin Description

Pin Number	Pin Name	Pin Function
1	FB	Analog Input. Feedback voltage for the APC loop op-amp. Polarity and scale are programmable via the APC configuration bits I OEMCFG1. Connect to V_{BIAS} if APC is not used.
2	VMPD	Analog Input. Multiplexed A/D converter input for monitoring transmitted optical power via a monitor photodiode. In most applications, VMPD will be connected directly to FB. The input range is 0 - V_{REF} or 0 - V_{REF}/4 depending upon the setting of the APC configuration bits
3	GNDA	Ground return for analog functions.
4	VDDA	Power supply input for analog functions.
5	VILD–	Analog Input. Reference terminal for the multiplexed pseudo-differential A/D converter inputs for monitoring laser bias current via a sense resistor (VILD+ is the sensing input). Tie to V_{DD} or GND to reference the voltage sensed on VILD+ to V_{DD} or GND, respectively.
6	VILD+	Analog Input. Multiplexed A/D input for monitoring laser bias current via a sense resistor (signal input); accommodates inputs referenced to V_{DD} or GND (see pin 5 description).
7	SHDN/TXFIN	Digital output/Input; programmable polarity. When used as shutdown output (SHDN), OEMCFG3 bit 2 set to 0, SHDN is asserted at the detection of a fault condition if OEMCFG4 bit 7 is set to 0. If OEMCFG4 bit 7 is set to 1, a fault condition will not assert SHDN. When programmed as TXFIN, it is an input for external fault signals to be ORed with the internal fault sources to drive TXFAULT.
8	VRX	Analog Input. Multiplexed A/D converter input for monitoring received optical power. The input range is 0 to V_{REF}. A 5-bit programmable EEPOT on this pin provides coarse calibration and ranging of the RX power measurement.
9	RS1	Digital Input; Transmitter Rate Select Input; ORed with soft rate select bit SRS1 to determine the state of the TRSOUT pin. The state of this pin is always reflected in the RS1S bit.
10	TXFAULT	Digital Output; Open-Drain, with programmable polarity. If OEMCFG5 bit 4 is set to 0, a high level indicates a hardware fault impeding transmitter operation. If OEMCFG5 bit 4 is set to 1, a low level indicates a hardware fault impeding transmitter operation. The state of this pin is always reflected in the TXFLT bit.
11	TXDISABLE	Digital input; Active high. The transmitter is disabled when this input is high or the STXDIS bit is set to 1. The state of this input is always reflected in the TXDIS bit.
12	DATA	Digital I/O, open-drain, bi-directional serial data input/output.
13	CLK	Digital input. Serial clock input.
14	VIN/INT	If bit 4 (IE) in the USRCTL register is set to 0 (its default value), this pin is configured as an analog input. If IE bit is set to 1, this pin is configured as an open-drain output. Analog input: Multiplexed A/D input for monitoring supply voltage, with a 0V to 5.5V input range. Open-drain output: outputs the internally generated active-low interrupt signal /INT.
15	RS0	Digital input. Receiver Rate Select input. ORed with soft rate select bit SRS0 to determine the state of the RRSOUT pin. The state of this pin is always reflected in the RS0S bit.
16	GNDD	Ground return for digital functions.
17	QGPO	Open-drain output. Can be selected (via OEMCFG3 bit 7) to be an open-drain GPO or an active-low, open-drain, pulsed reset signal output controlled by the status of bits [0-2] of byte A2h: FFh.
18	VDDD	Power supply input for digital functions.
19	RXLOS/ TRSOUT	Digital output. This programmable polarity, open-drain outputs has two purposes: If OEMCFG6 bit 2 = 0, indicates the loss of the received signal as indicated by a level of received optical power below the programmed RXLOS comparator threshold; may be wire-ORed with external signals. Normal operation is indicated by a low level when OEMCFG6 bit 3 is set to 0 and a high level when OEMCFG6 bit 3 is set to 1. RXLOS is de-asserted when VRX > LOSFLTn. The LOS bit reflects the state of RXLOS whether driven by the MIC3003 or an external circuit. If OEMCFG6 bit 2 = 1, TRSOUT is selected. This signal represents the transmitter rate select as per the SFF specification. This output is controlled by the SRS1 bit ORed with the RS1 input.
20	RRSOUT/ GPO	Digital Output. Open-Drain or push-pull. If OEMCFG3 bit 4 is set to 0, RRSOUT is selected. It represents the receiver rate select as per SFF. This output is controlled by the SRS0 bit ORed with RS0 input and is open drain only. If OEMCFG3 bit 4 is set to 1, GPO is selected. General-purpose, non-volatile output, it is controlled by the GPO configuration bits in OEMCFG3.
21	COMP	Analog output. Compensation terminal for the APC loop. Connect a capacitor between this pin and GNDA or V_{DDA} with the appropriate value to tune the APC loop time constant to a desirable value.
22	VBIAS	Analog output. Buffered DAC output capable of sourcing or sinking up to 10mA under control of the APC function to drive an external transistor or the APCSET pin of a laser diode driver for laser diode DC bias. The output and feedback polarity are programmable to accommodate either an NPN or a PNP transistor to drive a common-anode or common-cathode laser diode.
23	VMOD–	Analog input. This pin is the inverting terminal of the VMOD buffer op-amp. Connect to VMOD (gain = 1) or a feedback resistor network to set a different gain value.
24	VMOD	Analog Output. Buffered DAC output to set the modulation current on the laser driver IC. Operates with either a 0– V_{REF} or a (V_{DD}–V_{REF}) – V_{DD} output swing so as to generate either a ground-referenced or a V_{DD} referenced programmed voltage. A simple external circuit can be used to generate a programmable current for those drivers that require a current rather than a voltage input.

Absolute Maximum Ratings[1]

Power Supply Voltage, V_{DD} ..... +3.8V
Voltage on CLK, DATA, TXFAULT, VIN, RXLOS, TXDISABLE, RS0, RS1 ..... –0.3V to +6.0V
Voltage On Any Other Pin ..... –0.3V to V_{DD}+0.3V
Power Dissipation, T_A = 85°C 1.5W
Junction Temperature (T_J) ..... 150°C
Storage Temperature (T_S) ..... –65°C to +150°C
Soldering (20 sec.) ..... 260°C
ESD Ratings[3]
Human Body Model 2kV
Machine Model 300V

Operating Ratings[2]

Power Supply Voltage, V_{DDA}/V_{DDD} ..... +3.0V to +3.6V
Ambient Temperature Range (T_A) ..... –40°C to +105°C
Package Thermal Resistance
MLF® (θ_{JA}) ..... 43°C/W

Electrical Characteristics

For typical values, T_A = 25°C, V_{DDA} = V_{DDD} = +3.3V, unless otherwise noted. **Bold** values are guaranteed for +3.0V ≤ (V_{DDA} = V_{DDD}) ≤ 3.6V, $T_{(min)} \le T_A \le T_{(max)}$. [8]

Symbol	Parameter	Condition	Min	Typ	Max	Units
Power Supply						
I_{DD}	Supply Current	CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE low; all DACs at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
		CLK = DATA = V_{DDD} = V_{DDA}; TXDISABLE high; FLTDAC at full-scale; all A/D inputs at full-scale; all other pins open.		2.3	3.5	mA
V_{POR}	Power-on Reset Voltage	All registers reset to default values; A/D conversions initiated.		2.9	2.98	V
V_{UVLO}	Under-Voltage Lockout Threshold	Note 5	2.5	2.73		V
V_{HYST}	Power-on Reset Hysteresis Voltage			170		mV
t_{POR}	Power-on Reset Time	$V_{DD} > V_{POR}$, Note 4		50		µs
V_{REF}	Reference Voltage		1.210	1.225	1.240	V
$\Delta V_{REF}/\Delta V_{DDA}$	Voltage Reference Line Regulation			1.7		mV/V
Temperature-to-Digital Converter Characteristics						
	Local Temperature Measurement Error	–40°C ≤ T_A ≤ +105°C, Note 6		±1	±3	°C
t_{CONV}	Conversion Time	Note 4			60	ms
t_{SAMPLE}	Sample Period				100	ms
Voltage-to-Digital Converter Characteristics (V_{RX}, V_{AUX}, V_{BIAS}, V_{MPD}, V_{ILD}±)						
	Voltage Measurement Error	–40°C ≤ T_A ≤ +105°C, Note 6		±1	±2.0	%fs
t_{CONV}	Conversion Time	Note 4			10	ms
t_{SAMPLE}	Sample Period	Note 4			100	ms

Notes:

1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
4. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.
5. The MIC3003 will attempt to enter its shutdown state when V_{DD} falls below V_{UVLO}. This operation requires time to complete. If the supply voltage falls too rapidly, the operation may not be completed.
6. Does not include quantization error.

Voltage Input, V_{IN} (Pin 14 used as an ADC Input)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IN}	Input Voltage Range	–0.3 V ≤ V_{DD} ≤ 3.6V	GNDA		5.5	V
I_{LEAK}	Input Current	V_{IN} = V_{DD} or GND; V_{AUX} = V_{IN}		55		µA
C_{IN}	Input Capacitance			10		pF

Digital-to-Voltage Converter Characteristics (V_{MOD}, V_{BIAS})

	Accuracy	–40°C ≤ T_A ≤ +105°C, Note 7		±1	2.0	%fs
t_{CONV}	Conversion Time	Note 8			20	ms
DNL	Differential Non-linearity Error	Note 8		±0.5	±1	LSB

Bias Current Sense Inputs, V_{ILD}+, V_{ILD}–

V_{ILD}	Differential Input Signal Range, $\lvert V_{ILD}^+ - V_{ILD}^- \rvert$		0		V_{REF}/4	mV
I_{IN+}	V_{ILD}^+ input current				±1	µA
I_{IN-}	V_{ILD}^- input current	V_{ILD}^- referred to V_{DDA}		+150		µA
	$\lvert V_{ILD}^+ - V_{ILD}^- \rvert$ = 0.3V	V_{ILD}^- referred to GND		-150		µA
C_{IN}	Input Capacitance			10		pF

APC Op Amp, FB, V_{BIAS}, COMP

GBW	Gain Bandwidth Product	C_{COMP} = 20pF; Gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient[4]			1		µV/°C
V_{OUT}	Output Voltage Swing	I_{OUT} = 10mA, SRCE bit = 1	GNDA		1.25	V
		I_{OUT} = -10mA, SRCE bit = 0	V_{DDA} -1.25		V_{DDA}	V
I_{SC}	Output Short-Circuit Current			55		mA
t_{SC}	Short Circuit Withstand Time	$T_J \le 150°C$, Note 8				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; gain = 1, to GND		55		dB
		C_{COMP} = 20pF; gain = 1, to V_{DD}		40		
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF, note 8			1	V/V
$\Delta V/\Delta t$	Slew Rate	C_{COMP} = 20pF; gain = 1		3		V/µs
ΔRFB	Internal Feedback Resistor Tolerance			±20		%
ΔRFB/Δt	Internal Feedback Resistor Temperature Coefficient			25		ppm/C
I_{START}	Laser Start-up Current Magnitude	START = 01_h		0.375		mA
		START = 02_h		0.750		mA
		START = 04_h		1.500		mA
		START = 08_h		3.000		mA
C_{IN}	Pin Capacitance			10		pF

Notes:

7. Does not include quantization error.
8. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{MOD} Buffer Op-Amp, VMOD, V_{MOD}–						
GBW	Gain Bandwidth	C_{COMP} = 20pF; gain = 1		1		MHz
TC_{VOS}	Input Offset Voltage Temperature Coefficient			1		µV/°C
I_{BIAS}	V_{MOD}– Input Current			±0.1	±1	µA
V_{OUT}	Output Voltage Swing	I_{OUT} = ±1mA	GNDA+75		V_{DDA}-75	mV
I_{SC}	Output Short-Circuit Current			35		mA
t_{SC}	Short Circuit Withstand Time	T_J ≤ 150°C, Note 9				sec
PSRR	Power Supply Rejection Ratio	C_{COMP} = 20pF; gain = 1, to GND		65		dB
		C_{COMP} = 20pF; gain = 1, to V_{DD}		44		dB
A_{MIN}	Minimum Stable Gain	C_{COMP} = 20pF			1	V/V
ΔV/ΔT	Slew Rate	C_{COMP} = 20pF; gain = 1		1		V/µs
C_{IN}	Pin Capacitance			10		pF
Control and Status I/O, TXDISABLE, TXFAULT, RS0, RRSOUT(GPO), SHDN(TXFIN), RXLOS(TRSOUT), /INT, RS1, QGPO						
V_{IL}	Low Input Voltage				0.8	V
V_{IH}	High Input Voltage		2.0			V
V_{OL}	Low Output Voltage	I_{OL} ≤ 3mA			0.3	V
V_{OH}	High Output Voltage (applies to SHDN only)	I_{OH} ≤ 3mA			V_{DDD}-0.3	V
I_{LEAK}	Input Current				±1	µA
C_{IN}	Input Capacitance			10		pF
Transmit Optical Power Input, V_{MPD}						
V_{IN}	Input Voltage Range	Note 9	GNDA		V_{DDA}	V
V_{RX}	Input Signal Range	BIASREF=0			V_{REF}	V
		BIASREF=1	V_{DDA}–V_{REF}		V_{DDA}	V
C_{IN}	Input Capacitance	Note 9		10		pF
I_{LEAK}	Input Current				±1	µA
Received Optical Power Input, VRX, RXPOT						
	Input Voltage Range	Note 9	GNDA		V_{DDA}	V
V_{RX}	Valid Input Signal Range (ADC Input Range)		0		V_{REF}	V
$R_{RXPOT(32)}$	End-to-End Resistance	RXPOT = $1F_h$		32		KΩ
ΔRXPOT	Resistor Tolerance			±20		%
ΔRXPOT/ΔT	Resistor Temperature Coefficient			25		ppm/°C
$\Delta V_{RX}/V_{RXPOT}$	Divider Ratio Accuracy	00 ≤ RXPOT ≤ $1F_h$	-5		+5	%
I_{LEAK}	Input Current	RXPOT = 0 (disconnected)			±1	µA
C_{IN}	Input Capacitance	Note 9		10		pF
I_{LEAK}	Input Current				±1	µA

Note:
9. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.

Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
Control and Status I/O Timing, TXFAULT, TXDISABLE, RS0, RRSOUT, and RXLOS						
t_{OFF}	TXDISABLE Assert Time	From input asserted to optical output at 10% of nominal, C_{COMP} = 10nF.			**10**	µs
t_{ON}	TXDISABLE De-assert Time	From input de-asserted to optical output at 90% of nominal, C_{COMP} = 10nF.			**1**	ms
t_{INIT}	Initialization Time	From power on or transmitter enabled to optical output at 90% of nominal and TX_FAULT de-asserted. Note 10			**300**	ms
t_{INIT2}	Power-on Initialization Time	From power on to APC loop-enabled.			**200**	ms
t_{FAULT}	TXFAULT Assert Time	From fault condition to TXFAULT assertion. Note 10			95	µs
t_{RESET}	Fault Reset Time	Length of time TXDISABLE must be asserted to reset fault condition.	**10**			µs
t_{LOSS_ON}	RXLOS Assert Time	From loss of signal to RXLOS asserted.			95	µs
t_{LOSS_OFF}	RXLOS De-assert Time	From signal acquisition to LOS de-asserted.			**100**	µs
t_{DATA}	Analog Parameter Data Ready	From power on to valid analog parameter data available. Note 10			**400**	ms
t_{PROP_IN}	TXFAULT, TXDISABLE, RXLOS, RS0, RS1 Input Propagation Time	Time from input change to corresponding internal register bit set or cleared. Note 10			**1**	µs
t_{PROP_OUT}	TXFAULT, TRSOUT, TRRSOUT, /INT, QGPO Output Propagation Time	From an internal register bit set or cleared to corresponding output change. Note 10			**1**	µs
Fault Comparators						
FLTTMR	Fault Suppression Timer Clock Period	Note 10	**0.475**	0.5	**0.525**	ms
	Accuracy		-3		+3	%/fs
t_{REJECT}	Glitch Rejection	Maximum length pulse that will not cause output to change state. Note 10	4.5			µs
V_{SAT}	Saturation Detection Threshold	High level		95		%VDDA
		Low level		5		%VDDA
Power-On Hour Meter						
	Timebase Accuracy	0°C ≤ T_A ≤ +70°, Note 10	**+5**		**-5**	%
		–40°C ≤ T_A ≤ +105°C	**+10**		**-10**	%
	Resolution	Note 10		10		hours
Non-Volatile (FLASH) Memory						
t_{WR}	Write Cycle Time, Note 11	Measured from the SMBus STOP condition of a one-byte to eight-byte write transaction. Note 10			**13**	ms
	NVRAM Data Retention		**100**			years
Endurance	Maximum permitted number of write cycles to any single NVRAM location		**10,000**			cycles

Notes:
10. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.
11. The MIC3003 will not respond to serial bus transactions during an EEPROM write cycle. The host will receive a NACK response during t_{WR}.

Address(s)		Field Size (Bytes)	Name	Description
Hex	Dec			
00-3F	0-63	64	BIASLUT1	First 64 entries of the bias current temperature compensation LUT (Look-up Table) The additional 12 entries are located in A6: 58h – 63h.
40-7F	64-127	64	MODLUT1	First 64 entries of the modulation current temperature compensation LUT. The additional 12 entries are located in A6:.64h – 6Fh.
80-BF	128-191	64	IFTLUT1	First 64 entries of the bias current fault threshold temperature compensation LUT. The additional 12 entries are located in A6: 70h - 7Bh.
C0-FF	192-255	64	HATLUT1	First 64 entries of the bias current high alarm threshold temperature compensation LUT. The additional 12 entries are located in A6: 7C-87h.

Table 3. MIC3003 Serial Interface Address Map (Temperature Compensation Tables), Device Address = $A4_h$

Address(s)		Field Size (Bytes)	Name	Description
Hex	Dec			
00	0	1	OEMCFG0	OEM configuration register 0
01	1	1	OEMCFG1	OEM configuration register 1
02	2	1	OEMCFG2	OEM configuration register 2
03	3	1	APCSET0	APC setpoint register 0
04	4	1	APCSET1	APC setpoint register 1
05	5	1	APCSET2	APC setpoint register 2
06	6	1	MODSET0	Modulation setpoint register 0
07	7	1	IBFLT	Bias current fault-comparator threshold. This register is temperature compensated.
08	8	1	TXPFLT	TX power fault threshold
09	9	1	LOSFLT	RX LOS fault-comparator threshold
0A	10	1	FLTTMR	Fault comparator timer setting
0B	11	1	FLTMSK	Fault source mask bits
0C-0F	12-15	4	OEMPWSET	Password for access to OEM areas
10	16	1	OEMCAL0	OEM calibration register 0
11	17	1	OEMCAL1	OEM calibration register 1
12	18	1	LUTINDX	Look-up table index read-back
13	19	1	OEMCFG3	OEM configuration register 3
14	20	1	APCDAC	Reads back current APC DAC value (setpoint+offset)
15	21	1	MODDAC	Reads back current modulation DAC value (setpoint+offset)
16	22	1	OEMREAD	Reads back OEM calibration data
17	23	1	LOSFLTn	LOS deassert threshold
18	24	1	RXPOT	RXPOT tap selection
19	25	1	OEMCFG4	OEM configuration register 4
1A	26	1	OEMCFG5	OEM configuration register 5
1B	27	1	OEMCFG6	OEM configuration register 6
1C-1D	28-29	2	SCRATCH	Reserved – do not write; reads undefined.
1E	30	1	MODSET 1	Modulation setpoint register 1

Serial Data I/O Pin, Data

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OL}	Low Output Voltage	I_{OL} = 3mA			**0.4**	V
		I_{OL} = 6mA			**0.6**	V
V_{IL}	Low Input Voltage				**0.8**	V
V_{IH}	High Input Voltage		**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 12		10		pF

Serial Clock Input, CLK

V_{IL}	Low Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V			**0.8**	V
V_{IH}	High Input Voltage	2.7V ≤ V_{DD} ≤ 3.6V	**2.1**			V
I_{LEAK}	Input Current				**±1**	µA
C_{IN}	Input Capacitance	Note 12		10		pF

Serial Interface Timing[4]

t_1	CLK (clock) Period		**2.5**			µs
t_2	Data In Setup Time to CLK High		**100**			ns
t_3	Data Out Stable After CLK Low		**300**			ns
t_4	Data Low Setup Time to CLK Low	Start Condition	**100**			ns
t_5	Data High Hold Time After CLK High	Stop Condition	**100**			ns
t_{DATA}	Data Ready Time	From power on to completion of one set of ADC conversions; analog data available via serial interface.			**400**	ms

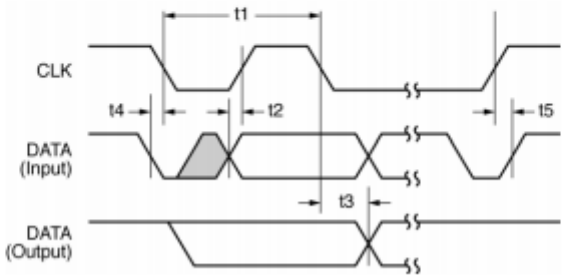
QGPO Reset Pulse Timing

t_1	QGPO reset pulse low duration	OEMCFG3 bit 7 = 1 A2h:255 (FFh) [2-0] switch to 111	**112.5**	125	137.5	µs
t_2	QGPO reset de-assertion to the clearing of A2:FFh bits 2:0	OEMCFG3 bit 7 = 1 A2h:255 (FFh) [2-0] ≠ 111	**20.25**	22.5	24.75	ms

Note:

12. Guaranteed by design and/or testing of related parameters. Not 100% tested in production.

Serial Interface Timing Diagram



Serial Interface Timing

Block Diagram

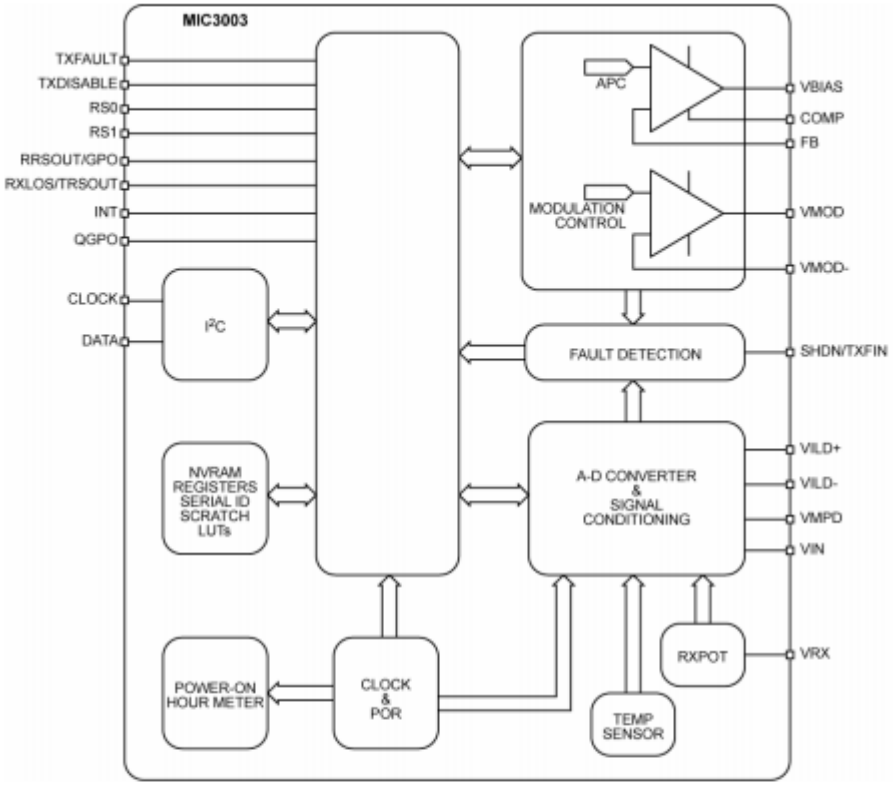


Figure 1. MIC3003 Block Diagram

Analog-to-Digital Converter/Signal Monitoring

A block diagram of the monitoring circuit is shown below. Each of the five analog parameters monitored by the MIC3003 is sampled in sequence. All five parameters are sampled and the results updated within the t_{CONV} duration given in the "Electrical Characteristics" section. In OEM mode, the channel that is normally used to measure V_{IN} may be assigned to measure the level of the V_{DDA} pin or one of five other nodes. This provides a kind of analog loopback for debug and test purposes. The V_{AUX} bits in OEMCFG0 control which voltage source is being sampled. The various V_{AUX} channels are level-shifted differently depending on the signal source, resulting in different LSB values and signal ranges. See Table 5.

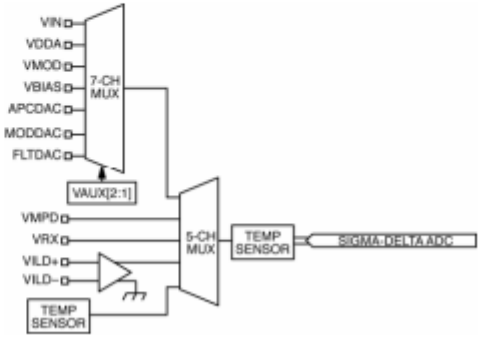


Figure 2. Analog-to-Digital Converter Block Diagram

Serial Interface Address Maps

Address (Decimal)	Field Size (Bytes)	Name	Description
0 –95	96	Serial ID defined by SFP MSA	General-purpose NVRAM; R/W under valid OEM password.
96 – 127	32	Vendor Specific	Vendor specific EEPROM
128 – 255	128	Reserved	Reserved for future use. General-purpose NVRAM; R/W under valid OEM password.

Table 1. MIC3003 Serial Interface Address Map, Device Address = $A0_h$

Address(s)		Field Size (Bytes)	Name	Description
Hex	Dec			
00-27	0-39	40	Alarm and Warning Thresholds	High/low limits for warnings and alarms; writeable using the OEM password; read-only otherwise.
28-37	40-55	16	Reserved	Reserved – do not write; reads undefined.
38-5B	56-91	36	Calibration Constants	Numerical constants for external calibration; writeable using the OEM password; read-only otherwise.
5C-5E	92-94	3	Reserved	Reserved – do not write; reads undefined.
5F	95	1	Checksum	General-purpose NVRAM; writeable using the OEM password; read-only otherwise.
60-69	96-105	10	Analog Data	Real time analog parameter data.
6A-6D	106-109	4	Reserved	Reserved – do not write; reads undefined.
6E	110	1	Control/Status Register	Control and status bits.
6F	111	1	Rate Select Control	Bits [7-6] control the use of the RS0 and RS1 inputs and the SRS0 and SRS1 register bits.
70-71	112-113	2	Alarm Flags	Alarm status bits; read-only.
72-73	114-115	2	Reserved	Reserved – do not write; reads undefined.
74-75	116-117	2	Warning Flags	Warning status bits; read-only.
76	118	1	Extended Control/Status Register	Additional control and status bits.
77	119	1	Reserved	Reserved – do not write; reads undefined.
78-7E	120-126	7	OEMPW	OEM password entry field. The four-byte OEM password location can be selected to be 78h-7Bh (120-123) by setting OEMCFG5 bit 2 to 0 (default) or 7Bh-7Eh (123-126) by setting OEMCFG5 bit 2 to a one.
7F	127	1	Vendor-specific	Vendor specific. Reserved – do not write; reads undefined.
80-F7	128-247	120	User Scratchpad	User-writeable EEPROM. General-purpose NVRAM.
F8-F9	248-249	2	Alarms Masks	Bit = 0: Corresponding alarm not masked. Bit = 1: Corresponding alarm masked.
FA-FB	250-251	2	Warnings Masks	Bit = 0: Corresponding warning not masked. Bit = 1: Corresponding warning masked.
FC-FD	252-253	2	Reserved	Reserved – do not write; reads undefined.
FE	254	1	USRCTL	End-user control and status bits.
FF	255	1	RESETOUT	Bits [2:0] of this register control the QGPO reset output (pin 17) If OEMCFG3 bit 7 is set to 1.

Table 2. MIC3003 Serial Interface Address Map, Device Address = A2

Address(s)		Field Size (Bytes)	Name	Description
HEX	DEC			
1F	31	1	MODSET 2	Modulation setpoint register 2
20-27	32-39	8	POHDATA	Power-on hour meter scratchpad
28-47	40-71	32	RXLUT	RX power internal calibration coefficient table. Eight sets of slope and offset coefficients provide a piecewise-linear transfom for the receive power ADC result.
48-57	72-87	16	CALCOEF	Slope and offset coefficients used for temperature, voltage, bias current, and transmit power internal calibration
58-63	88-99	12	IFTLUT2	Additional 12 entries of the bias current fault threshold temperature compensation LUT.
64-6F	100-111	12	BIASLUT2	Additional 12 entries of the bias current temperature compensation LUT.
70-7B	112-123	12	MODLUT2	Additional 12 entries of the modulation current temperature compensation LUT.
7C-87	124-135	12	HATLUT2	Additional 12 entries of the bias current high alarm threshold temperature compensation LUT.
88-CF	136-207	72	SCRATCH	OEM scratchpad area
D0-DD	208-221	14	RXLUTSEG/ SCRATCH	Receive power calibration segment delimiters. Each of the eight segments can have its own slope and offset coefficient. Used to refine the shape of the piecewise-linear function used for receive power in internal calibration mode. These bytes may also be part of the OEM scratch pad if the hard coded delimiters option is selected, see the description of OEMCFG6
DE-FA	222-250	29	SCRATCH	OEM scratchpad area
FB-FC	251-252	2	POH	Power on hour meter result; read-only
FD	253	1	Data Ready Flags	Data ready bits for each measured parameter; read-only
FE	254	1	MFG_ID	Manufacturer identification (Micrel's manufacturer ID is 42, 2Ah)
FF	255	1	DEV_ID	Device ID and die revision

Table 4. MIC3003 Serial Interface Address Map (OEM Configuration Registers), Device Address = $A6_h$

Channel	ADC Resolution (bits)	Conditions	Input Range (V)	LSB[1]
TEMP	8 or 9		N/A	1°C or 0.5°C
VAUX	8	See Table 6		
VMPD	8	GAIN = 0; BIASREF = 0	GNDA - V_{REF}	4.77mV
		GAIN = 0; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF})	
		GAIN = 1; BIASREF = 0	GNDA - V_{REF}/4	1.17mV
		GAIN = 1; BIASREF = 1	V_{DDA} – (V_{DDA} – V_{REF}/4)	
VILD	8	VILD- = VDDA	V_{DDA} – (V_{DDA} – V_{REF})	4.77mV
		VILD- = GNDA	GNDA - V_{REF}	
VRX	12	RXPOT = 00	0 - V_{REF}	0.298mV

Table 5. A/D Input Signal Ranges and Resolutions

Note:

1. Assumes typical VREF value of 1.22V.

Channel	VAUX [2:0]	Input Range (V)	LSB[1] (mV)
V_{IN}	000 = 00_h	0.5V to 5.5V	25.6mV
V_{DDA}	001 = 01_h	0.5V to 5.5V	25.6mV
V_{BIAS}	010 = 02_h	0.5V to 5.5V	25.6mV
V_{MOD}	011 = 03_h	0.5V to 5.5V	25.6mV
APCDAC	100 = 04_h	0V to V_{REF}	4.77mV
MODDAC	101 = 05_h	0V to V_{REF}	4.77mV
FLTDAC	110 = 06_h	0V to V_{REF}	4.77mV

Table 6. V_{AUX} Input Signal Ranges and Resolutions

Note:

1. Assumes typical V_{REF} value of 1.22V.

Alarms and Warnings Interrupt Source Masking

Alarm and warning violations set the flags in the Alarm and Warning Status Registers, and also assert the interrupt output if they are not masked. If an alarm or warning is masked, it will not set the interrupt. Table 8 shows the locations of the masking bits. The warning or alarm is masked if the corresponding bit is set to 1.