Quad-Channel Digital Isolators

ADuM1400/ADuM1401/ADuM1402

FEATURES

- Low power operation
  - 5 V operation
    - 1.0 mA per channel max @ 0 Mbps to 2 Mbps
    - 3.5 mA per channel max @ 10 Mbps
    - 31 mA per channel max @ 90 Mbps
  - 3 V operation
    - 0.7 mA per channel max @ 0 Mbps to 2 Mbps
    - 2.1 mA per channel max @ 10 Mbps
    - 20 mA per channel max @ 90 Mbps
- Bidirectional communication
- 3 V/5 V level translation
- High temperature operation: 105°C
- High data rate: dc to 90 Mbps (NRZ)
- Precise timing characteristics
  - 2 ns max pulse-width distortion
  - 2 ns max channel-to-channel matching
- High common-mode transient immunity: >25 kV/µs
- Output enable function
- Wide body 16-lead SOIC package, Pb-free models available
- Safety and regulatory approvals
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - CSA component acceptance notice #5A
  - VDE certificate of conformity
    - DIN EN 60747-5-2 (VDE 0884 Part 2): 2003-01
    - DIN EN 60950 (VDE 0805): 2001-12; EN 60950: 2000
    - V_{IORM} = 560 V peak

APPLICATIONS

- General-purpose multichannel isolation
- SPI® interface/data converter isolation
- RS-232/RS-422/RS-485 transceiver
- Industrial field bus isolation

GENERAL DESCRIPTION

The ADuM140x are 4-channel digital isolators based on Analog Devices' *i*Coupler® technology. Combining high speed CMOS and monolithic air core transformer technology, these isolation components provide outstanding performance characteristics superior to alternatives such as optocoupler devices.

By avoiding the use of LEDs and photodiodes, *i*Coupler devices remove the design difficulties commonly associated with optocouplers. The typical optocoupler concerns regarding uncertain current transfer ratios, nonlinear transfer functions, and temperature and lifetime effects are eliminated with the simple *i*Coupler digital interfaces and stable performance characteristics. The need for external drivers and other discretes is eliminated with these *i*Coupler products. Furthermore, *i*Coupler devices consumes one-tenth to one-sixth the power of optocouplers at comparable signal data rates.

The ADuM140x isolators provide four independent isolation channels in a variety of channel configurations and data rates (see the Ordering Guide). All models operate with the supply voltage on either side ranging from 2.7 V to 5.5 V, providing compatibility with lower voltage systems as well as enabling a voltage translation functionality across the isolation barrier. In addition, the ADuM140x provides low pulse-width distortion (<2 ns for CRW grade) and tight channel-to-channel matching (<2 ns for CRW grade). Unlike other optocoupler alternatives, the ADuM140x isolators have a patented refresh feature that ensures dc correctness in the absence of input logic transitions and during power-up/power-down conditions.

FUNCTIONAL BLOCK DIAGRAMS

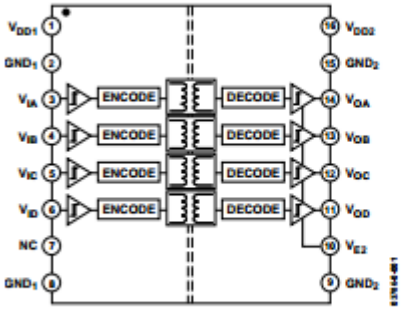

Figure 1. ADuM1400 Functional Block Diagram

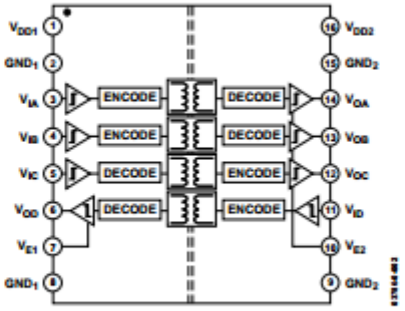

Figure 2. ADuM1401 Functional Block Diagram

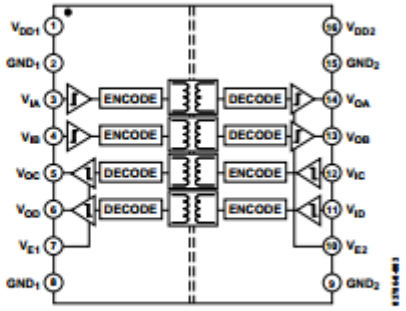

Figure 3. ADuM1402 Functional Block Diagram

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5/04—Data Sheet Changed from Rev. 0 to Rev. A.

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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION[1]

4.5 V ≤ V_{DD1} ≤ 5.5 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 5 V.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI(Q)}$		0.50	0.53	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$		0.19	0.21	mA	
ADuM1400, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		2.2	2.8	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		0.9	1.4	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		8.6	10.6	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1(90)}$		76	100	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(90)}$		21	25	mA	45 MHz logic signal freq.
ADuM1401, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$		1.8	2.4	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1(10)}$		7.1	9.0	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(10)}$		4.1	5.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1(90)}$		62	82	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(90)}$		35	43	mA	45 MHz logic signal freq.
ADuM1402, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1(Q)}$, $I_{DD2(Q)}$		1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1(10)}$, $I_{DD2(10)}$		5.6	7.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1(90)}$, $I_{DD2(90)}$		49	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	$0 \le V_{IA}$, V_{IB}, V_{IC}, $V_{ID} \le V_{DD1}$ or V_{DD2}, $0 \le V_{E1}$, $V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	2.0			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.8	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}, V_{DD2} − 0.1	5.0		V	I_{Ox} = −20 μA, V_{Ix} = V_{IxH}
		V_{DD1}, V_{DD2} − 0.4	4.8		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 μA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 μA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50	65	100	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels
ADuM140xBRW						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	32	50	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			15	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width[3]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	18	27	32	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			10	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		2.5		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.2		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$		0.19		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDO(D)}$		0.05		mA/Mbps	

See Notes on next page.

ELECTRICAL CHARACTERISTICS—3 V OPERATION[1]

2.7 V ≤ V_{DD1} ≤ 3.6 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.0 V.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI (Q)}$		0.26	0.31	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO (Q)}$		0.11	0.14	mA	
ADuM1400, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.5	0.9	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		1.4	2.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		42	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		11	15	mA	45 MHz logic signal freq.
ADuM1401, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$		0.7	1.2	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$		3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$		2.2	3.0	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$		34	52	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$		19	27	mA	45 MHz logic signal freq.
ADuM1402, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (Q)}$, $I_{DD2 (Q)}$		0.9	1.5	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (10)}$, $I_{DD2 (10)}$		3.0	4.2	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)						
V_{DD1} or V_{DD2} Supply Current	$I_{DD1 (90)}$, $I_{DD2 (90)}$		27	39	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	μA	$0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID} \le V_{DD1}$ or V_{DD2}, $0 \le V_{E1}, V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}	1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}			0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}, V_{DD2} − 0.1	3.0		V	$I_{Ox} = -20$ μA, $V_{Ix} = V_{IxH}$
		V_{DD1}, V_{DD2} − 0.4	2.8		V	$I_{Ox} = -4$ mA, $V_{Ix} = V_{IxH}$
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	$I_{Ox} = 20$ μA, $V_{Ix} = V_{IxL}$
			0.04	0.1	V	$I_{Ox} = 400$ μA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{Ox} = 4$ mA, $V_{Ix} = V_{IxL}$
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width[3]	PW			1000	ns	$C_L = 15$ pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	$C_L = 15$ pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50	75	100	ns	$C_L = 15$ pF, CMOS signal levels
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[5]	PWD			40	ns	$C_L = 15$ pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	$C_L = 15$ pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	$C_L = 15$ pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xBRW						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	38	50	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width[3]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	34	45	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\|t_{PLH} - t_{PHL}\|$[5]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			16	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low-to-High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F		3		ns	C_L = 15 pF, CMOS signal levels
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		1.1		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$		0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDO(D)}$		0.03		mA/Mbps	

ELECTRICAL CHARACTERISTICS—MIXED 5 V/3 V OR 3 V/5 V OPERATION[1]

5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 2.7 V ≤ V_{DD2} ≤ 3.6 V; 3 V/5 V operation: 2.7 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V; all min/max specifications apply over the entire recommended operation range, unless otherwise noted; all typical specifications are at T_A = 25°C; V_{DD1} = 3.0 V, V_{DD2} = 5 V; or V_{DD1} = 5 V, V_{DD2} = 3.0 V.

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, per Channel, Quiescent	$I_{DDI(Q)}$					
5 V/3 V Operation			0.50	0.53	mA	
3 V/5 V Operation			0.26	0.31	mA	
Output Supply Current, per Channel, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.11	0.14	mA	
3 V/5 V Operation			0.19	0.21	mA	
ADuM1400, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1(Q)}$					
5 V/3 V Operation			2.2	2.8	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.2	1.9	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2(Q)}$					
5 V/3 V Operation			0.5	0.9	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.4	mA	DC to 1 MHz logic signal freq.

10 Mbps (BRW and CRW Grades Only)					
V_{DD1} Supply Current	$I_{DD1 (10)}$				
5 V/3 V Operation		8.6	10.6	mA	5 MHz logic signal freq.
3 V/5 V Operation		4.5	6.5	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$				
5 V/3 V Operation		1.4	2.0	mA	5 MHz logic signal freq.
3 V/5 V Operation		2.6	3.5	mA	5 MHz logic signal freq.
90 Mbps (CRW Grade Only)					
V_{DD1} Supply Current	$I_{DD1 (90)}$				
5 V/3 V Operation		76	100	mA	45 MHz logic signal freq.
3 V/5 V Operation		42	65	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$				
5 V/3 V Operation		11	15	mA	45 MHz logic signal freq.
3 V/5 V Operation		21	25	mA	45 MHz logic signal freq.
ADuM1401, Total Supply Current, Four Channels[2]					
DC to 2 Mbps					
V_{DD1} Supply Current	$I_{DD1 (Q)}$				
5 V/3 V Operation		1.8	2.4	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation		1.0	1.6	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$				
5 V/3 V Operation		0.7	1.2	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation		1.2	1.8	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)					
V_{DD1} Supply Current	$I_{DD1 (10)}$				
5 V/3 V Operation		7.1	9.0	mA	5 MHz logic signal freq.
3 V/5 V Operation		3.7	5.4	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$				
5 V/3 V Operation		2.2	3.0	mA	5 MHz logic signal freq.
3 V/5 V Operation		4.1	5.0	mA	5 MHz logic signal freq.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			62	82	mA	45 MHz logic signal freq.
3 V/5 V Operation			34	52	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			19	27	mA	45 MHz logic signal freq.
3 V/5 V Operation			35	43	mA	45 MHz logic signal freq.
ADuM1402, Total Supply Current, Four Channels[2]						
DC to 2 Mbps						
V_{DD1} Supply Current	$I_{DD1 (Q)}$					
5 V/3 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (Q)}$					
5 V/3 V Operation			0.9	1.5	mA	DC to 1 MHz logic signal freq.
3 V/5 V Operation			1.5	2.1	mA	DC to 1 MHz logic signal freq.
10 Mbps (BRW and CRW Grades Only)						
V_{DD1} Supply Current	$I_{DD1 (10)}$					
5 V/3 V Operation			5.6	7.0	mA	5 MHz logic signal freq.
3 V/5 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (10)}$					
5 V/3 V Operation			3.0	4.2	mA	5 MHz logic signal freq.
3 V/5 V Operation			5.6	7.0	mA	5 MHz logic signal freq.

90 Mbps (CRW Grade Only)						
V_{DD1} Supply Current	$I_{DD1 (90)}$					
5 V/3 V Operation			49	62	mA	45 MHz logic signal freq.
3 V/5 V Operation			27	39	mA	45 MHz logic signal freq.
V_{DD2} Supply Current	$I_{DD2 (90)}$					
5 V/3 V Operation			27	39	mA	45 MHz logic signal freq.
3 V/5 V Operation			49	62	mA	45 MHz logic signal freq.
For All Models						
Input Currents	I_{IA}, I_{IB}, I_{IC}, I_{ID}, I_{E1}, I_{E2}	−10	+0.01	+10	µA	$0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID} \le V_{DD1}$ or V_{DD2}, $0 \le V_{E1}, V_{E2} \le V_{DD1}$ or V_{DD2}
Logic High Input Threshold	V_{IH}, V_{EH}					
5 V/3 V Operation		2.0			V	
3 V/5 V Operation		1.6			V	
Logic Low Input Threshold	V_{IL}, V_{EL}					
5 V/3 V Operation				0.8	V	
3 V/5 V Operation				0.4	V	
Logic High Output Voltages	V_{OAH}, V_{OBH}, V_{OCH}, V_{ODH}	V_{DD1}/ V_{DD2} − 0.1	V_{DD1}/V_{DD2}		V	I_{Ox} = −20 µA, V_{Ix} = V_{IxH}
		V_{DD1}/ V_{DD2} − 0.4	V_{DD1}/ V_{DD2} − 0.2		V	I_{Ox} = −4 mA, V_{Ix} = V_{IxH}
Logic Low Output Voltages	V_{OAL}, V_{OBL}, V_{OCL}, V_{ODL}		0.0	0.1	V	I_{Ox} = 20 µA, V_{Ix} = V_{IxL}
			0.04	0.1	V	I_{Ox} = 400 µA, V_{Ix} = V_{IxL}
			0.2	0.4	V	I_{Ox} = 4 mA, V_{Ix} = V_{IxL}
SWITCHING SPECIFICATIONS						
ADuM140xARW						
Minimum Pulse Width[3]	PW			1000	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		1			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	50	70	100	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[5]	PWD			40	ns	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			50	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching[7]	$t_{PSKCD/OD}$			50	ns	C_L = 15 pF, CMOS signal levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
ADuM140xBRW						
Minimum Pulse Width[3]	PW			100	ns	C_L = 15 pF,CMOS signal levels
Maximum Data Rate[4]		10			Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	15	35	50	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[5]	PWD			3	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			5		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			22	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			3	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			6	ns	C_L = 15 pF, CMOS signal levels
ADuM140xCRW						
Minimum Pulse Width[3]	PW		8.3	11.1	ns	C_L = 15 pF, CMOS signal levels
Maximum Data Rate[4]		90	120		Mbps	C_L = 15 pF, CMOS signal levels
Propagation Delay[5]	t_{PHL}, t_{PLH}	20	30	40	ns	C_L = 15 pF, CMOS signal levels
Pulse-Width Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[5]	PWD		0.5	2	ns	C_L = 15 pF, CMOS signal levels
Change vs. Temperature			3		ps/°C	C_L = 15 pF, CMOS signal levels
Propagation Delay Skew[6]	t_{PSK}			14	ns	C_L = 15 pF, CMOS signal levels
Channel-to-Channel Matching, Codirectional Channels[7]	t_{PSKCD}			2	ns	C_L = 15 pF, CMOS signal levels

Channel-to-Channel Matching, Opposing-Directional Channels[7]	t_{PSKOD}			5	ns	C_L = 15 pF, CMOS signal levels
For All Models						
Output Disable Propagation Delay (High/Low to High Impedance)	t_{PHZ}, t_{PLH}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Enable Propagation Delay (High Impedance to High/Low)	t_{PZH}, t_{PZL}		6	8	ns	C_L = 15 pF, CMOS signal levels
Output Rise/Fall Time (10% to 90%)	t_R/t_F					C_L = 15 pF, CMOS signal levels
5 V/3 V Operation			3.0		ns	
3 V/5 V Operation			2.5		ns	
Common-Mode Transient Immunity at Logic High Output[8]	$\|CM_H\|$	25	35		kV/µs	$V_{Ix} = V_{DD1}/V_{DD2}$, V_{CM} = 1000 V, transient magnitude = 800 V
Common-Mode Transient Immunity at Logic Low Output[8]	$\|CM_L\|$	25	35		kV/µs	V_{Ix} = 0 V, V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r					
5 V/3 V Operation			1.2		Mbps	
3 V/5 V Operation			1.1		Mbps	
Input Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$					
5 V/3 V Operation			0.19		mA/Mbps	
3 V/5 V Operation			0.10		mA/Mbps	
Output Dynamic Supply Current, per Channel[9]	$I_{DDI(D)}$					
5 V/3 V Operation			0.03		mA/Mbps	
3 V/5 V Operation			0.05		mA/Mbps	

ABSOLUTE MAXIMUM RATINGS

Ambient temperature = 25°C, unless otherwise noted.

Table 9.

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_{ST}	−65	+150	°C
Ambient Operating Temperature	T_A	−40	+105	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	−0.5	+7.0	V
Input Voltage[1, 2]	V_{IA}, V_{IB}, V_{IC}, V_{ID}, V_{E1}, V_{E2}	−0.5	V_{DDI} + 0.5	V
Output Voltage[1, 2]	V_{OA}, V_{OB}, V_{OC}, V_{OD}	−0.5	V_{DDO} + 0.5	V
Average Output Current, Per Pin[3]				
Side 1	I_{O1}	−18	+18	mA
Side 2	I_{O2}	−22	+22	mA
Common-Mode Transients[4]		−100	+100	kV/µs

PIN CONFIGURATIONS AND PIN FUNCTION DESCRIPTIONS

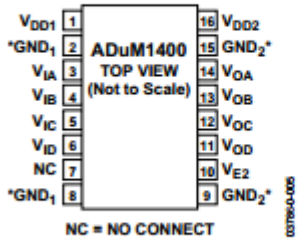

Figure 5. ADuM1400 Pin Configuration

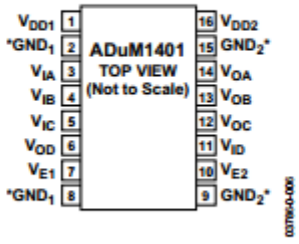

Figure 6. ADuM1401 Pin Configuration

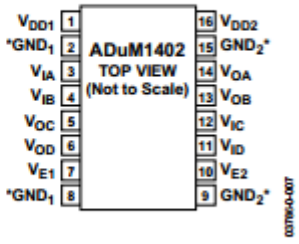

Figure 7. ADuM1402 Pin Configuration