TOSHIBA Field Effect Transistor Silicon P Channel MOS Type (L^2-π-MOSV)

2SJ401

DC−DC Converter, Relay Drive and Motor Drive Applications

- 4 V gate drive
- Low drain−source ON resistance : $R_{DS\ (ON)}$ = 33 mΩ (typ.)
- High forward transfer admittance : $|Y_{fs}|$ = 20 S (typ.)
- Low leakage current : I_{DSS} = −100 μA (max) (V_{DS} = −60 V)
- Enhancement−mode : V_{th} = −0.8~−2.0 V (V_{DS} = −10 V, I_D = −1 mA)

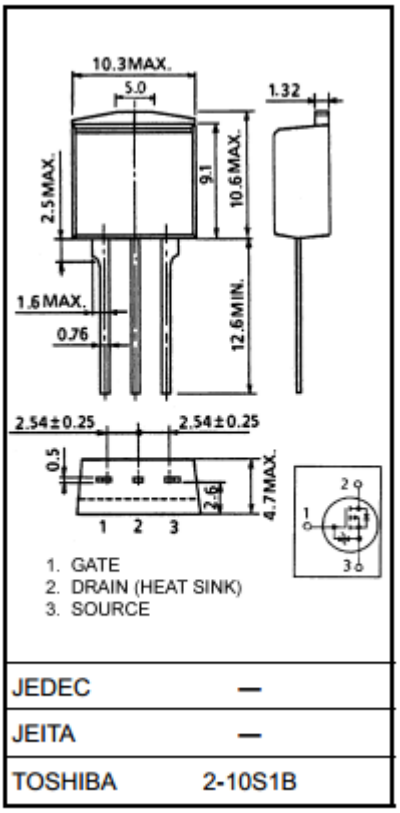
Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit
Drain−source voltage		V_{DSS}	−60	V
Drain−gate voltage (R_{GS} = 20 kΩ)		V_{DGR}	−60	V
Gate−source voltage		V_{GSS}	±20	V
Drain current	DC (Note 1)	I_D	−20	A
	Pulse(Note 1)	I_{DP}	−80	A
Drain power dissipation (Tc = 25°C)		P_D	100	W
Single pulse avalanche energy (Note 2)		E_{AS}	800	mJ
Avalanche current		I_{AR}	−20	A
Repetitive avalenche energy (Note 3)		E_{AR}	10	mJ
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55~150	°C

Thermal Characteristics

Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.25	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	83.3	°C / W

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-10S1B

Weight: 1.5 g (typ.)

Thermal Characteristics

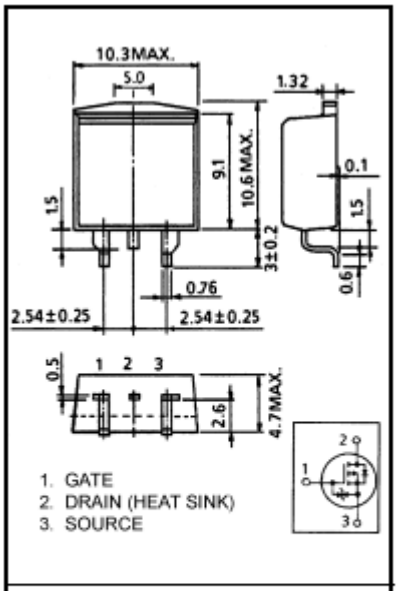
Characteristics	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th\ (ch-c)}$	1.25	°C / W
Thermal resistance, channel to ambient	$R_{th\ (ch-a)}$	83.3	°C / W

Note 1: Please use devices on condition that the channel temperature is below 150°C.

Note 2: V_{DD} = −50 V, T_{ch} = 25°C (initial), L = 1.44 mH, R_G = 25 Ω, I_{AR} = −20 A

Note 3: Repetitive rating: Pulse width limited by maximum channel temperature

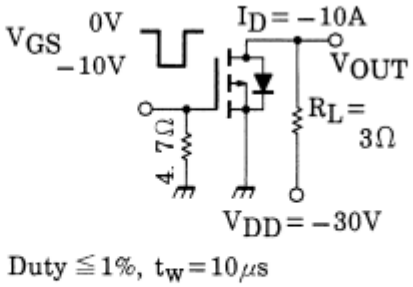
This transistor is an electrostatic sensitive device.
Please handle with caution.



JEDEC	—
JEITA	—
TOSHIBA	2-10S2B

Weight: 1.5 g (typ.)

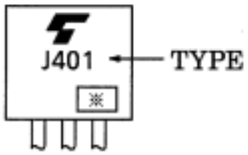
Electrical Characteristics (Ta = 25°C)

Characteristics		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V	—	—	±10	μA
Drain cut−off current		I_{DSS}	V_{DS} = −60 V, V_{GS} = 0 V	—	—	−100	μA
Drain−source breakdown voltage		$V_{(BR)\ DSS}$	I_D = −10 mA, V_{GS} = 0 V	−60	—	—	V
Gate threshold voltage		V_{th}	V_{DS} = −10 V, I_D = −1 mA	−0.8	—	−2.0	V
Drain−source ON resistance		$R_{DS\ (ON)}$	V_{GS} = −4 V, I_D = −10 A	—	50	90	mΩ
			V_{GS} = −10 V, I_D = −10 A	—	33	45	
Forward transfer admittance		$\|Y_{fs}\|$	V_{DS} = −10 V, I_D = −10 A	10	20	—	S
Input capacitance		C_{iss}	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz	—	2800	—	pF
Reverse transfer capacitance		C_{rss}		—	450	—	
Output capacitance		C_{oss}		—	1300	—	
Switching time	Rise time	t_r		—	15	—	ns
	Turn−on time	t_{on}		—	35	—	
	Fall time	t_f		—	25	—	
	Turn−off time	t_{off}		—	120	—	
Total gate charge (Gate−source plus gate−drain)		Q_g	V_{DD} ≈ −48 V, V_{GS} = −10 V, I_D = −20 A	—	90	—	nC
Gate−source charge		Q_{gs}		—	65	—	
Gate−drain ("miller") charge		Q_{gd}		—	25	—	

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	−20	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	−80	A
Forward voltage (diode)	V_{DSF}	I_{DR} = −20 A, V_{GS} = 0 V	—	—	1.7	V
Reverse recovery time	t_{rr}	I_{DR} = −20 A, V_{GS} = 0 V dI_{DR} / dt = 50 A / μs	—	75	—	ns
Reverse recovery charge	Qrr		—	83	—	nC

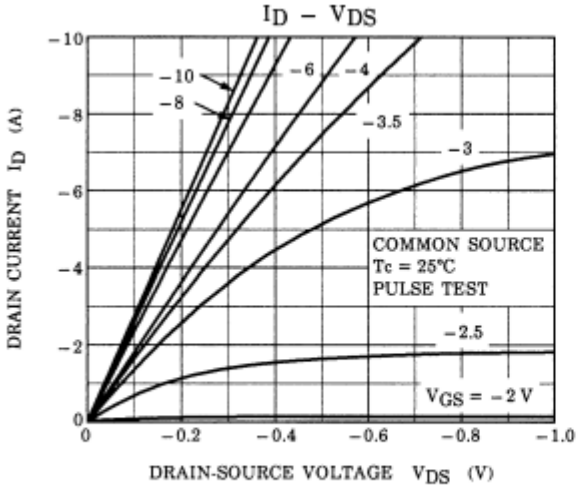
Marking

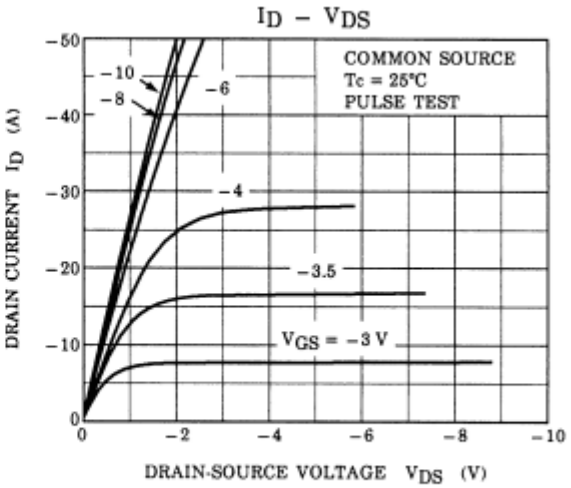


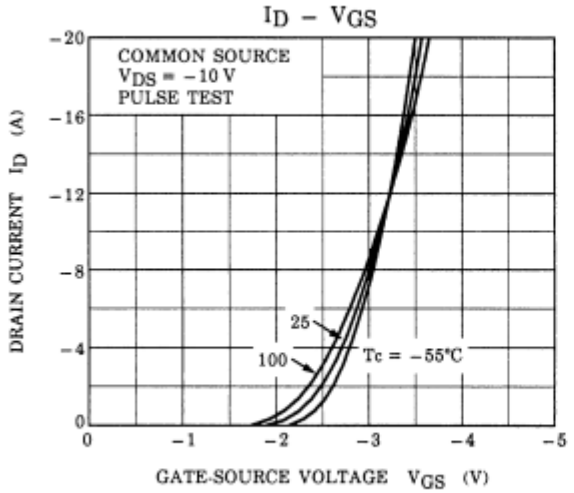
※ Lot Number

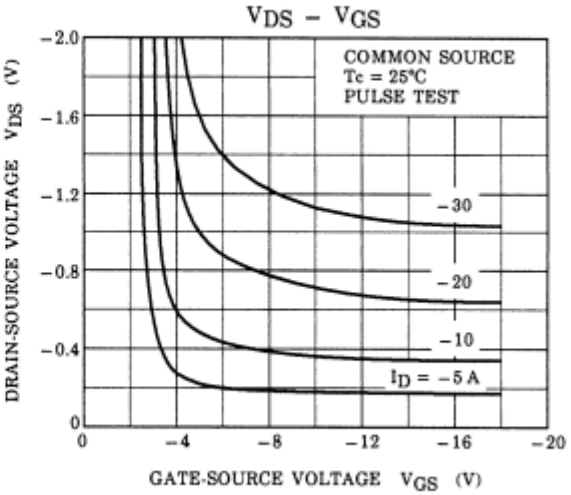
□□ — Month (Starting from Alphabet A)

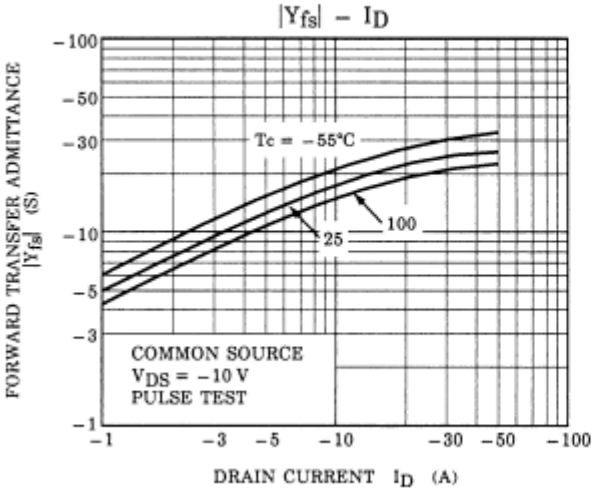
Year (Last Number of the Christian Era)

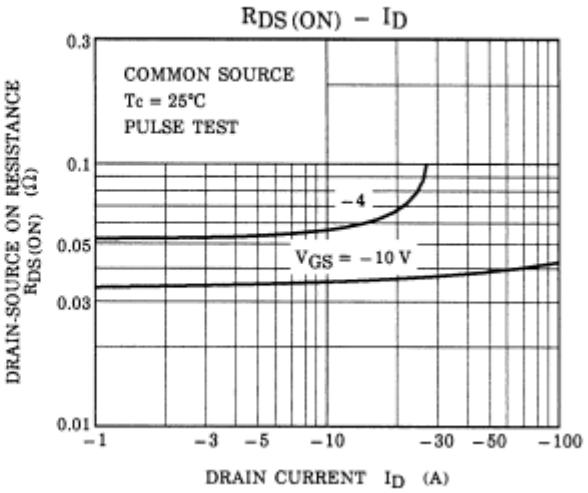


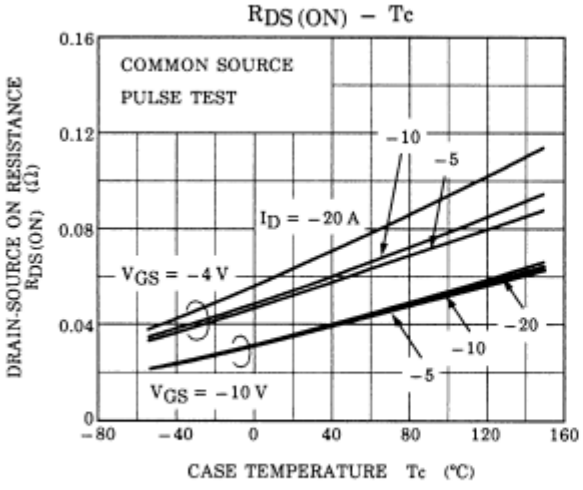


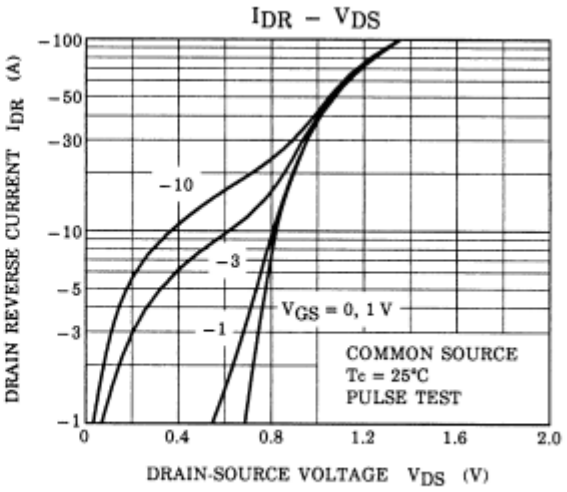


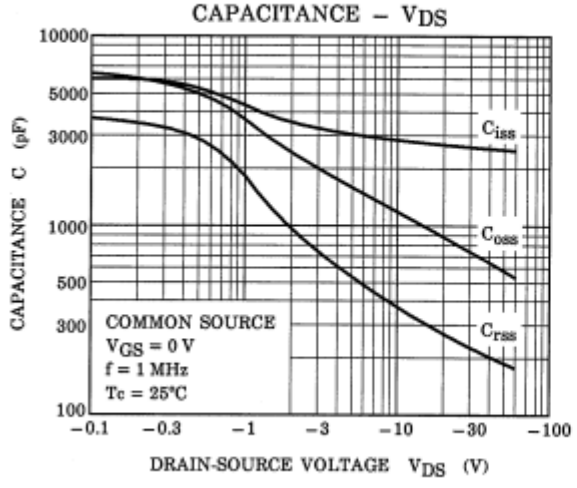


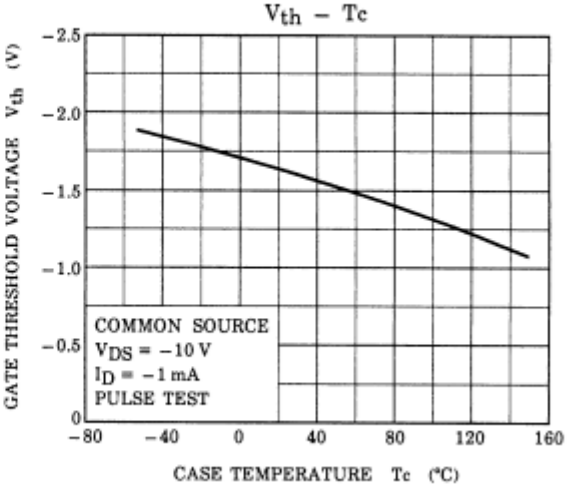

|Yfs| – ID
FORWARD TRANSFER ADMITTANCE |Yfs| (S)
DRAIN CURRENT ID (A)
Tc = −55°C
25
100
COMMON SOURCE
VDS = −10 V
PULSE TEST

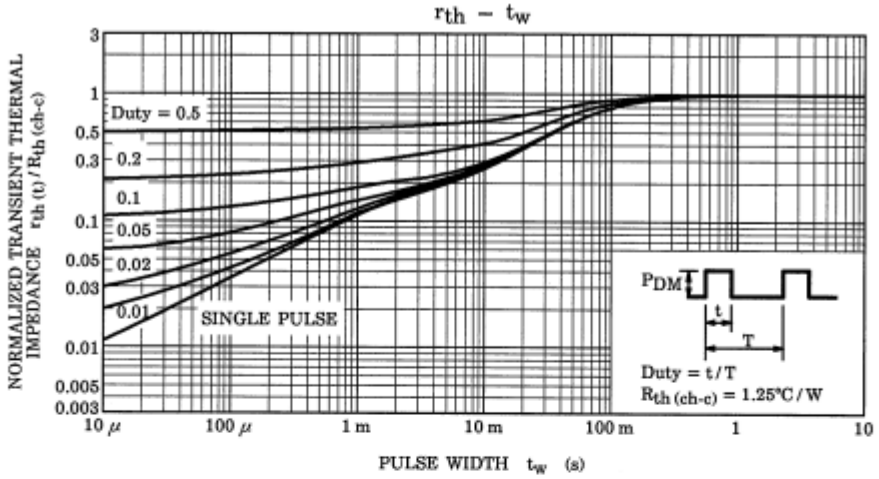

RDS (ON) – ID
DRAIN-SOURCE ON RESISTANCE RDS (ON) (Ω)
DRAIN CURRENT ID (A)
COMMON SOURCE
Tc = 25°C
PULSE TEST
−4
VGS = −10 V

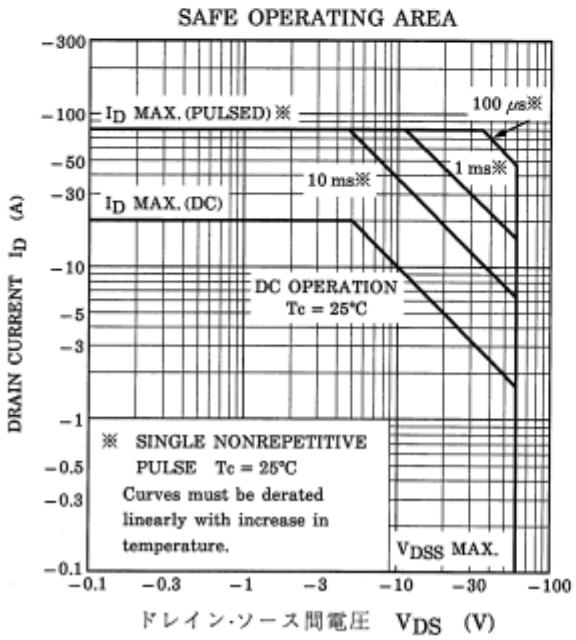

RDS (ON) – Tc
DRAIN-SOURCE ON RESISTANCE RDS (ON) (Ω)
CASE TEMPERATURE Tc (°C)
COMMON SOURCE
PULSE TEST
−10
−5
ID = −20 A
VGS = −4 V
−20
−10
−5
VGS = −10 V

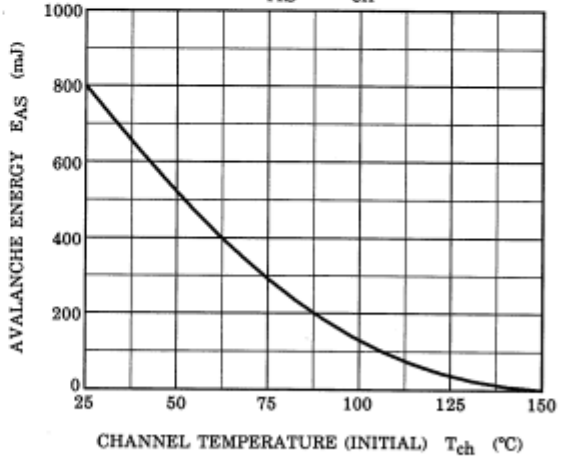

IDR – VDS
DRAIN REVERSE CURRENT IDR (A)
DRAIN-SOURCE VOLTAGE VDS (V)
−10
−3
−1
VGS = 0, 1 V
COMMON SOURCE
Tc = 25°C
PULSE TEST

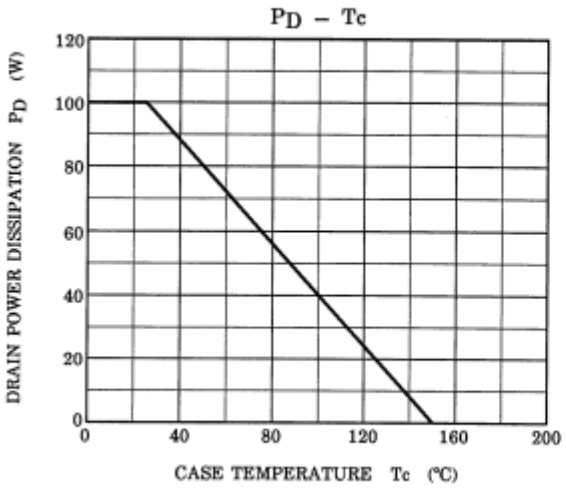

CAPACITANCE – VDS
CAPACITANCE C (pF)
DRAIN-SOURCE VOLTAGE VDS (V)
Ciss
Coss
Crss
COMMON SOURCE
VGS = 0 V
f = 1 MHz
Tc = 25°C

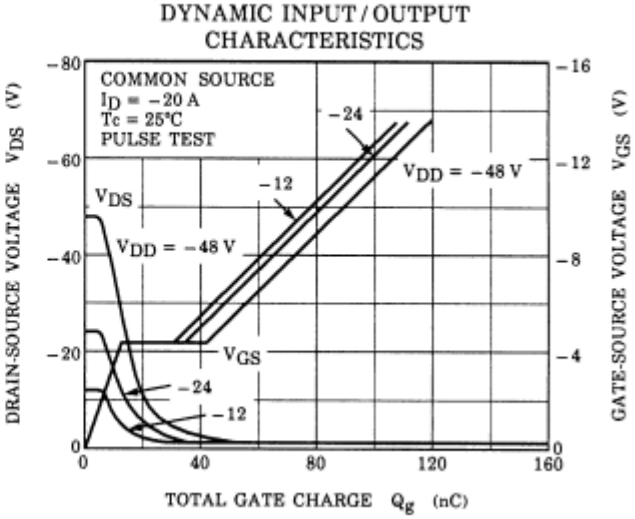

Vth – Tc
GATE THRESHOLD VOLTAGE Vth (V)
CASE TEMPERATURE Tc (°C)
COMMON SOURCE
VDS = −10 V
ID = −1 mA
PULSE TEST

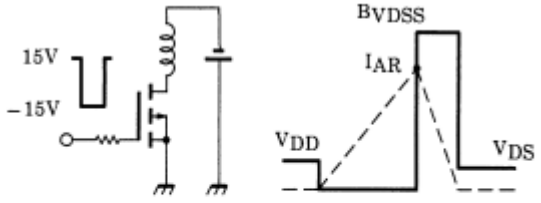

r_{th} – t_w
NORMALIZED TRANSIENT THERMAL IMPEDANCE $r_{th}(t)/R_{th(ch-c)}$
Duty = 0.5
0.2
0.1
0.05
0.02
0.01
SINGLE PULSE
P_{DM}
t
T
Duty = t/T
$R_{th(ch-c)}$ = 1.25°C/W
PULSE WIDTH t_w (s)


SAFE OPERATING AREA
DRAIN CURRENT I_D (A)
I_D MAX. (PULSED) ※
100 μs※
10 ms※
1 ms※
I_D MAX. (DC)
DC OPERATION
Tc = 25°C
※ SINGLE NONREPETITIVE PULSE Tc = 25°C
Curves must be derated linearly with increase in temperature.
V_{DSS} MAX.
ドレイン・ソース間電圧 V_{DS} (V)


E_{AS} – T_{ch}
AVALANCHE ENERGY E_{AS} (mJ)
CHANNEL TEMPERATURE (INITIAL) T_{ch} (°C)


P_D – Tc
DRAIN POWER DISSIPATION P_D (W)
CASE TEMPERATURE Tc (°C)


DYNAMIC INPUT/OUTPUT CHARACTERISTICS
COMMON SOURCE
I_D = −20 A
Tc = 25°C
PULSE TEST
V_{DS}
V_{DD} = −48 V
V_{GS}
−24
−12
DRAIN-SOURCE VOLTAGE V_{DS} (V)
GATE-SOURCE VOLTAGE V_{GS} (V)
TOTAL GATE CHARGE Q_g (nC)



TEST CIRCUIT WAVE FORM

$R_G = 25\Omega$
$V_{DD} = -50V$, $L = 1.44mH$

$$E_{AS} = \frac{1}{2} \cdot L \cdot I^2 \cdot \left(\frac{B_{VDSS}}{B_{VDSS} - V_{DD}} \right)$$