DC-to-2.5 GHz High IP3 Active Mixer

AD8343

FEATURES

High-performance active mixer
Broadband operation to 2.5 GHz
Conversion gain: 7 dB
Input IP3: 16.5 dBm
LO drive: −10 dBm
Noise figure: 14 dB
Input P_{1dB}: 2.8 dBm
Differential LO, IF and RF Ports
50 Ω LO input impedance
Single-supply operation: 5 V @ 50 mA typical
Power-down mode @ 20 µA typical

APPLICATIONS

Cellular base stations
Wireless LAN
Satellite converters
SONET/SDH radio
Radio links
RF instrumentation

FUNCTIONAL BLOCK DIAGRAM

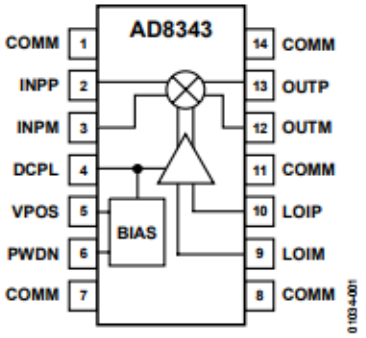

Figure 1.

GENERAL DESCRIPTION

The AD8343 is a high-performance broadband active mixer. With wide bandwidth on all ports and very low intermodulation distortion, the AD8343 is well suited for demanding transmit applications or receive channel applications.

The AD8343 provides a typical conversion gain of 7 dB. The integrated LO driver supports a 50 Ω differential input impedance with low LO drive level, helping to minimize external component count.

The open-emitter differential inputs can be interfaced directly to a differential filter or driven through a balun (transformer) to provide a balanced drive from a single-ended source.

The open-collector differential outputs can be used to drive a differential IF signal interface or convert to a single-ended signal through the use of a matching network or transformer. When centered on the VPOS supply voltage, the outputs swing ±1 V.

The LO driver circuitry typically consumes 15 mA of current. Two external resistors are used to set the mixer core current for required performance, resulting in a total current of 20 mA to 60 mA. This corresponds to power consumption of 100 mW to 300 mW with a single 5 V supply.

The AD8343 is fabricated on Analog Devices, Inc.'s high-performance 25 GHz silicon bipolar IC process. The AD8343 is available in a 14-lead TSSOP package. It operates over a −40°C to +85°C temperature range. A device-populated evaluation board is available.

SPECIFICATIONS

BASIC OPERATING INSTRUCTIONS

V_S = 5.0 V, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Conditions/Comments	Min	Typ	Max	Unit
INPUT INTERFACE (INPP, INPM)					
Differential Open Emitter					
DC Bias Voltage	Internally generated	1.1	1.2	1.3	V
Operating Current Each Input (I_O)	Current set by R3, R4; see Figure 72	5	17.6	20	mA
Value of Bias Setting Resistor[1]	1% bias resistors; R3, R4; see Figure 72		68.1		Ω
Port Differential Impedance	f = 50 MHz; R3 and R4 = 68.1 Ω; see Figure 57		5.6 + j 1.4		Ω
OUTPUT INTERFACE (OUTP, OUTM)					
Differential Open Collector					
DC Bias Voltage	Externally applied	4.5	5	5.5	V
Voltage Swing	Collector bias (V_S) = VPOS	1.65	V_S ± 1	V_S + 2	V
Operating Current Each Output	Same as input current		I_O		mA
Port Differential Impedance	f = 50 MHz; see Figure 60		900 − j 77		Ω
LO INTERFACE (LOIP, LOIM)					
Differential Common Base Stage					
DC Bias Voltage[2]	Internally generated; (port is typically ac-coupled)	300	360	450	mV
LO Input Power	50 Ω impedance; see Figure 65	−12	−10	−3	dBm
Port Differential Reflection Coefficient	See Figure 64		−10		dB
POWER-DOWN INTERFACE (PWDN)					
PWDN Threshold	Assured on			V_S − 1.5	V
	Assured off	V_S − 0.5			V
PWDN Response Time[3]	Time from device on to off; see Figure 52		2.2		µs
	Time from device off to on; see Figure 53		500		ns
PWDN Input Bias Current	PWDN = 0 V (device on)		−160	−250	µA
	PWDN = 5 V (device off)		0		µA
POWER SUPPLY					
Supply Voltage Range		4.5	5.0	5.5	V
Total Quiescent Current	R3 and R4 = 68.1 Ω; see Figure 72		50	60	mA
	Over temperature			75	mA
Powered-Down Current	V_S = 5.5 V		20	95	µA
	V_S = 4.5 V		6	15	µA
	Over temperature; V_S = 5.5 V		50	150	µA

[1] The balance in the bias current in the two legs of the mixer input is important to applications where a low feedthrough of the local oscillator (LO) is critical.
[2] This voltage is proportional to absolute temperature (PTAT). See the DC Coupling the LO section for more information regarding this interface.
[3] Response time until device meets all specified conditions.

TYPICAL AC PERFORMANCE

V_S = 5.0 V, T_A = 25°C; see Figure 72, Table 6 through Table 8.

Table 2.

Input Frequency (MHz)	Output Frequency (MHz)	Conversion Gain (dB)	SSB Noise Figure (dB)	Input IP3 (dBm)	Input 1 dB Compression Point (dBm)
RECEIVER CHARACTERISTICS					
400	70	5.6	10.5	20.5	3.3
900	170	3.6	11.4	19.4	3.6
1900	170	7.1	14.1	16.5	2.8
2400	170	6.8	15.3	14.5	2.1
2400	425	5.4	16.2	16.5	2.2
TRANSMITTER CHARACTERISTICS					
150	900	7.5	17.9	18.1	1.9
150	1900	0.25	16.0	13.4	0.8

TYPICAL ISOLATION PERFORMANCE

V_S = 5.0 V, T_A = 25°C; see Figure 72, Table 6 through Table 8.

Table 3.

Input Frequency (MHz)	Output Frequency (MHz)	LO to Output Leakage (dBm)	2xLO to Output Leakage (dBm)	3xLO to Output Leakage (dBm)	Input to Output Leakage (dBm)
RECEIVER CHARACTERISTICS					
400	70	−40.1	−51.0	−44.0	−62.4
900	170	−44.4	−35.5	<−75.0	−56.9
1900	170	−65.6	−38.3	−73.3	−65.7
2400	170	−66.7	−44.4	<−73.7	−73.7
2400	425	−51.1	−49.4	<−75.0	−92.3
TRANSMITTER CHARACTERISTICS					
150	900	−30	−32	−62	−50
150	1900	−25	−17	−65	−40

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
VPOS Quiescent Voltage	5.5 V
OUTP, OUTM Quiescent Voltage	5.5 V
INPP, INPM Voltage Differential (Either Polarity)	500 mV
LOIP, LOIM Current (Injection or Extraction)	1 mA
LOIP, LOIM Voltage Differential (Either Polarity)	500 mV
Internal Power Dissipation (TSSOP)[1]	320 mW
θ_{JA} (TSSOP)	125°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to + 85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering 60 sec)	300°C

[1] A portion of the device power is dissipated by external bias resistors, R3 and R4.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

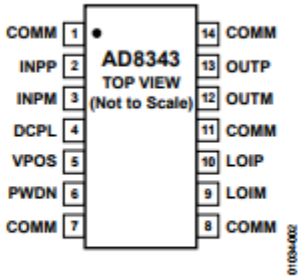

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 7, 8, 11, 14	COMM	Connect to low impedance circuit ground.
2	INPP	Differential Input Pin. This pin needs to be dc-biased and typically ac-coupled; see Figure 3.
3	INPM	Differential Input Pin. This pin needs to be dc-biased and typically ac-coupled; see Figure 3.
4	DCPL	Bias rail decoupling capacitor connection for LO driver; see Figure 6.
5	VPOS	Positive Supply Voltage (V_S), 4.5 V to 5.5 V. Ensure adequate supply bypassing for proper device operation as shown in the Applications section.
6	PWDN	Power-Down Interface. Connect pin to ground for normal operating mode. Connect pin to supply for power-down mode; see Figure 5.
9	LOIM	Differential Local Oscillator (LO) Input Pin. Typically ac-coupled; see Figure 4.
10	LOIP	Differential Local Oscillator (LO) Input Pin. Typically ac-coupled; see Figure 4.
12	OUTM	Open-Collector Differential Output Pin. This pin needs to be dc-biased and (usually) ac-coupled; see Figure 3.
13	OUTP	Open-Collector Differential Output Pin. This pin needs to be dc-biased and (usually) ac-coupled; see Figure 3.

SIMPLIFIED INTERFACE SCHEMATICS

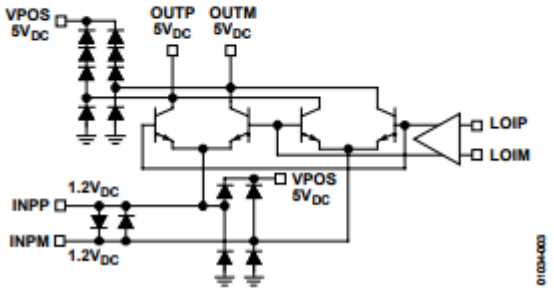

Figure 3. Input and Output Ports

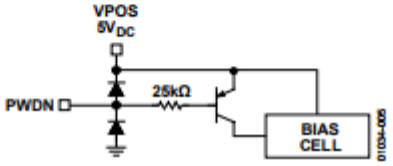

Figure 5. Power-Down Pin

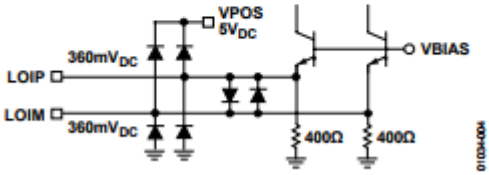

Figure 4. LO Port

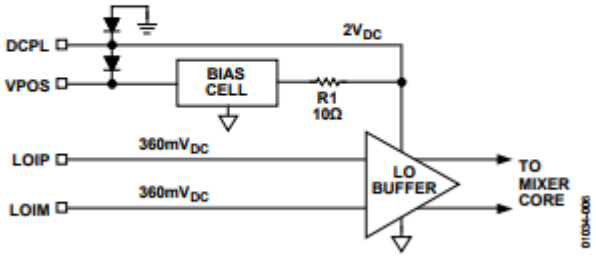

Figure 6. Bias Decoupling Pin

RECEIVER CHARACTERISTICS

f_{IN} = 400 MHz, f_{OUT} = 70 MHz, f_{LO} = 330 MHz, see Figure 72, Table 6, and Table 8.

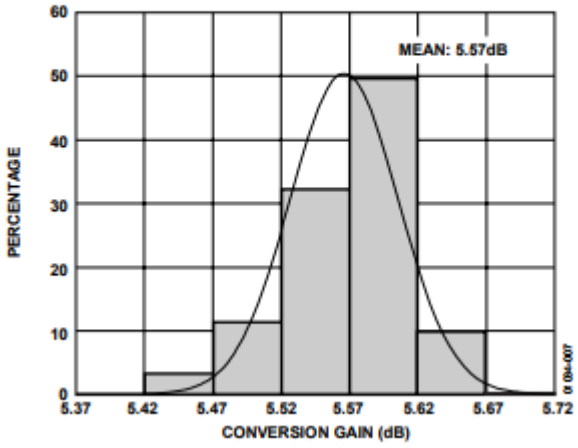

Figure 7. Gain Histogram; f_{IN} = 400 MHz, f_{OUT} = 70 MHz

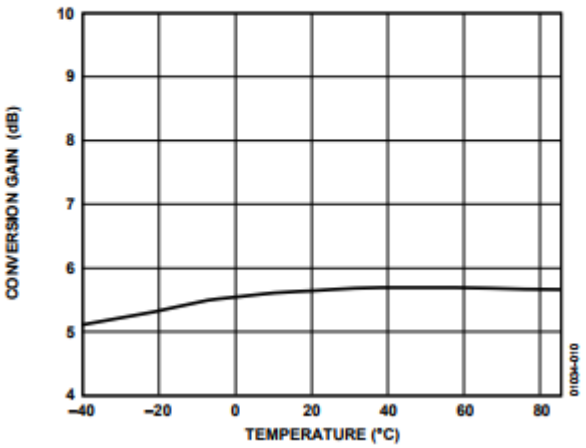

Figure 10. Gain Performance Over Temperature; f_{IN} = 400 MHz, f_{OUT} = 70 MHz

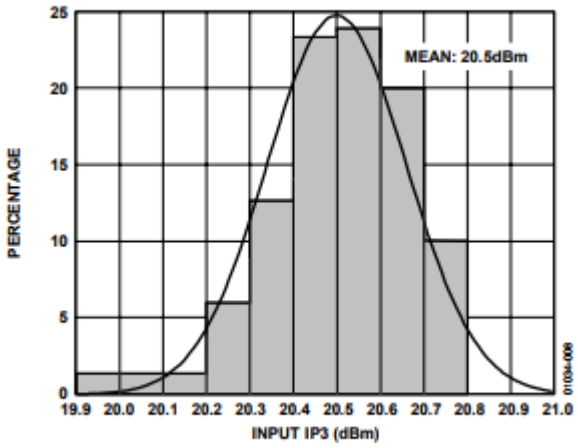

Figure 8. Input IP3 Histogram; f_{IN} = 400 MHz, f_{OUT} = 70 MHz

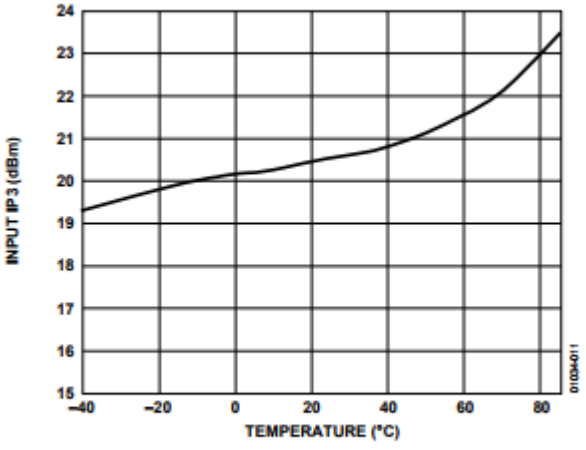

Figure 11. Input IP3 Performance Over Temperature; f_{IN} = 400 MHz, f_{OUT} = 70 MHz

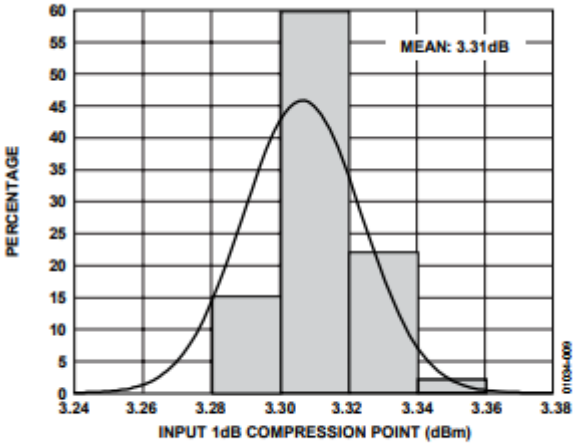

Figure 9. Input 1 dB Compression Point Histogram; f_{IN} = 400 MHz, f_{OUT} = 70 MHz

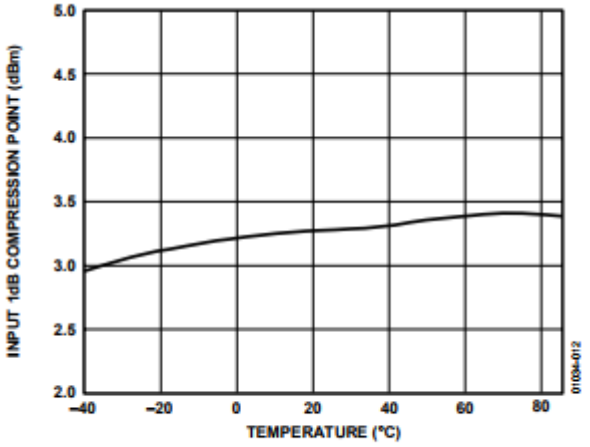

Figure 12. Input 1 dB Compression Point Performance Over Temperature; f_{IN} = 400 MHz, f_{OUT} = 70 MHz

f_{IN} = 900 MHz, f_{OUT} = 170 MHz, f_{LO} = 730 MHz, see Figure 72, Table 6, and Table 8.

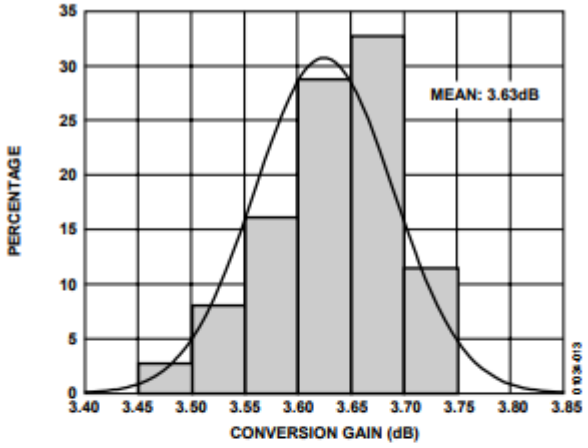

Figure 13. Gain Histogram; f_{IN} = 900 MHz, f_{OUT} = 170 MHz

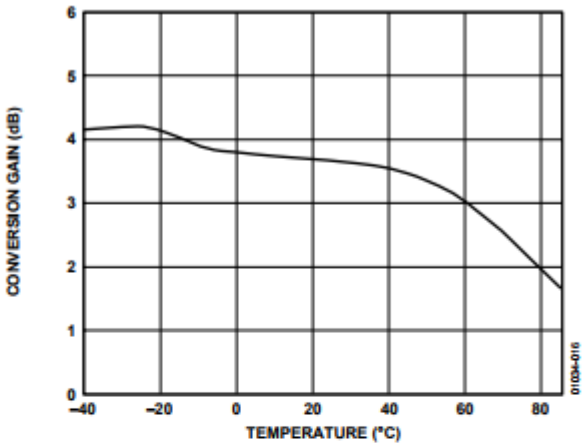

Figure 16. Gain Performance Over Temperature; f_{IN} = 900 MHz, f_{OUT} = 170 MHz

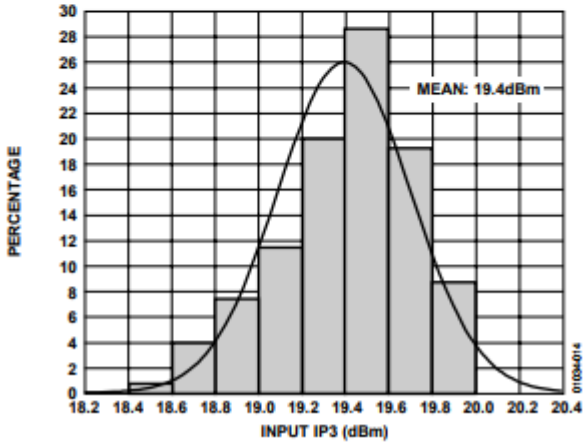

Figure 14. Input IP3 Histogram; f_{IN} = 900 MHz, f_{OUT} = 170 MHz

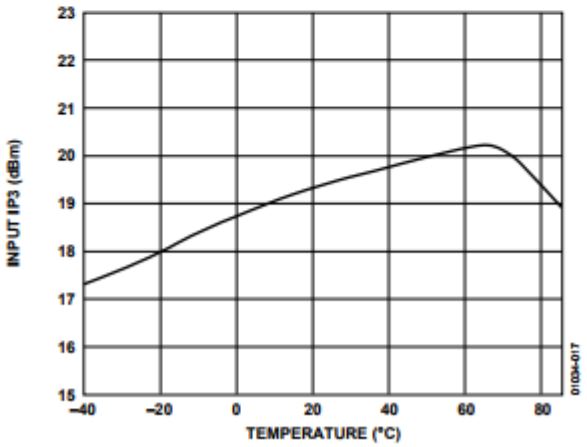

Figure 17. Input IP3 Performance Over Temperature; f_{IN} = 900 MHz, f_{OUT} = 170 MHz

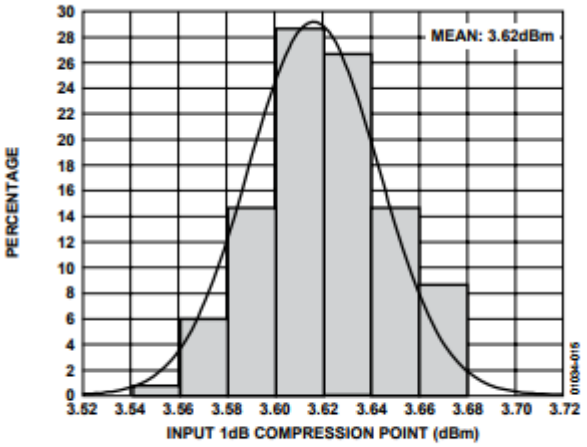

Figure 15. Input 1 dB Compression Point Histogram; f_{IN} = 900 MHz, f_{OUT} = 170 MHz

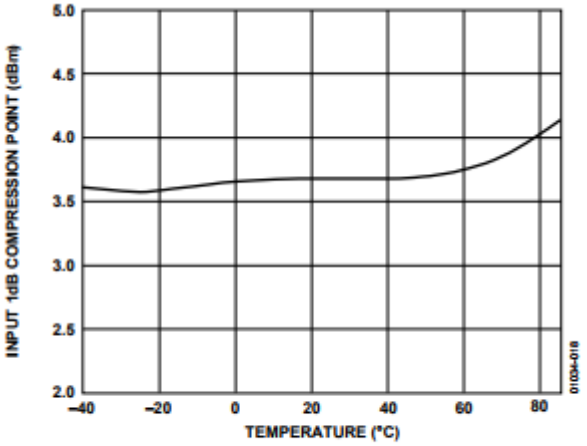

Figure 18. Input 1dB Compression Point Performance Over Temperature; f_{IN} = 900 MHz, f_{OUT} = 170 MHz

f_{IN} = 1900 MHz, f_{OUT} = 170 MHz, f_{LO} = 1730 MHz, see Figure 72, Table 6, and Table 8.

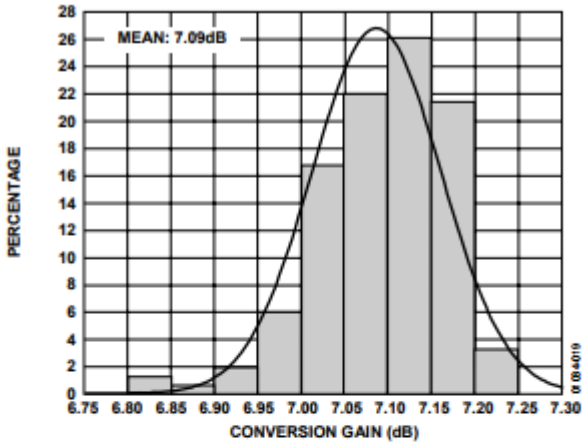

Figure 19. Gain Histogram; f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

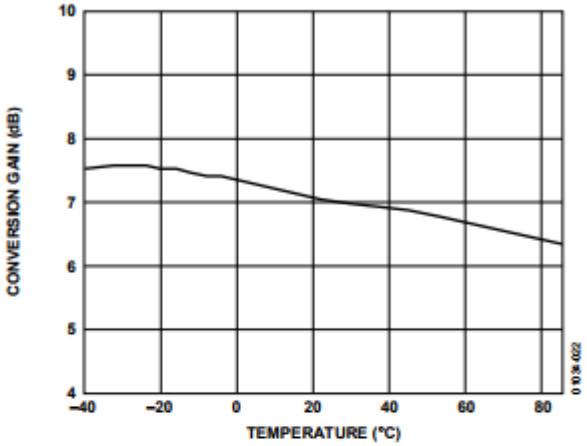

Figure 22. Gain Performance Over Temperature; f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

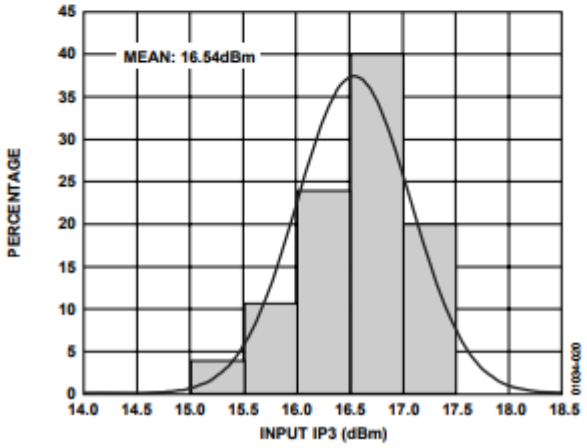

Figure 20. Input IP3 Histogram; f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

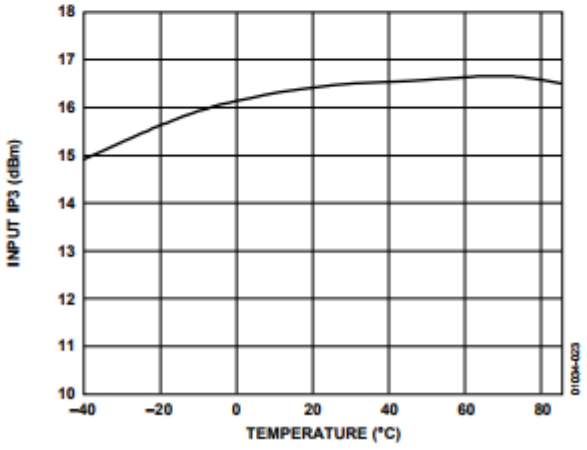

Figure 23. Input IP3 Performance Over Temperature; f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

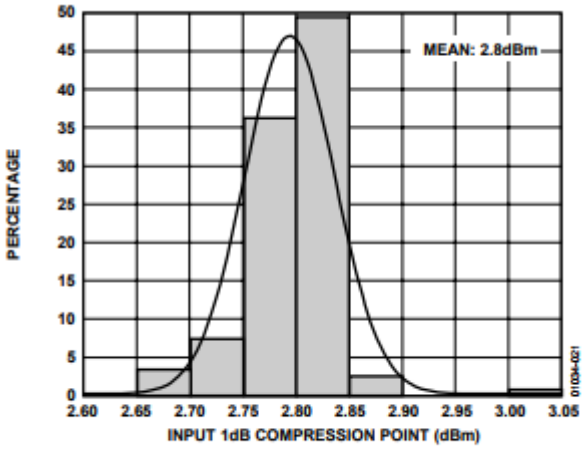

Figure 21. Input 1 dB Compression Point Histogram; f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

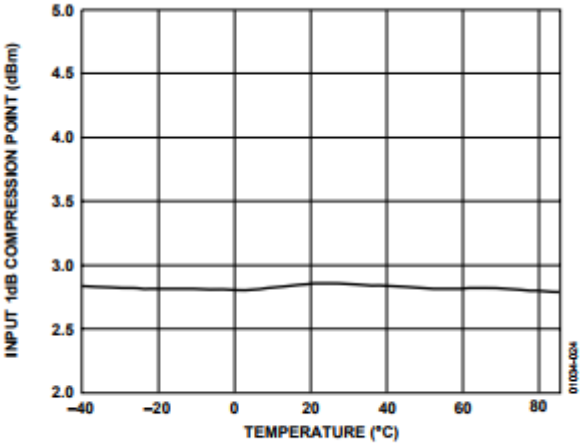

Figure 24. Input 1 dB Compression Point Performance Over Temperature; f_{IN} = 1900 MHz, f_{OUT} = 170 MHz

f_{IN} = 2400 MHz, f_{OUT} = 170 MHz, f_{LO} = 2230 MHz, see Figure 72, Table 6, and Table 8.

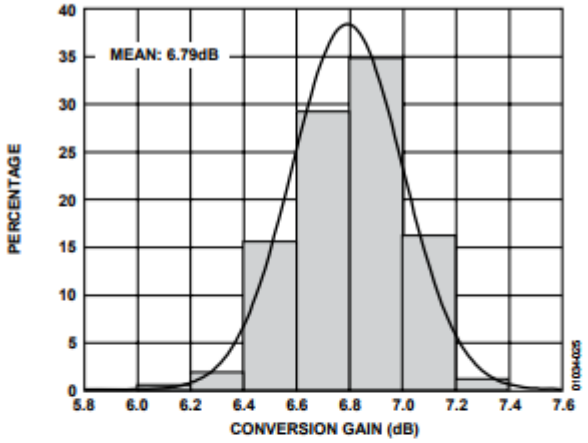

Figure 25. Gain Histogram; f_{IN} = 2400 MHz, f_{OUT} = 170 MHz

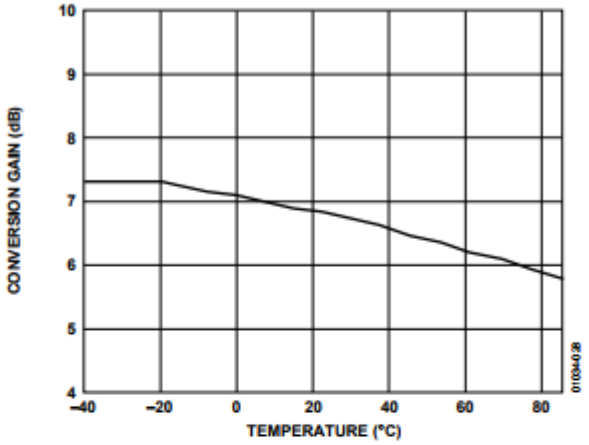

Figure 28. Gain Performance Over Temperature; f_{IN} = 2400 MHz, f_{OUT} = 170 MHz

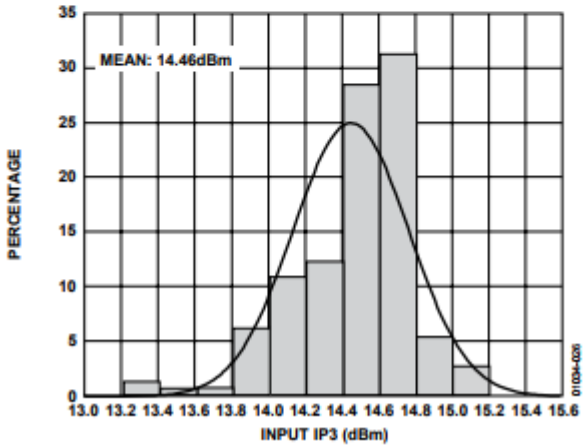

Figure 26. Input IP3 Histogram; f_{IN} = 2400 MHz, f_{OUT} = 170 MHz

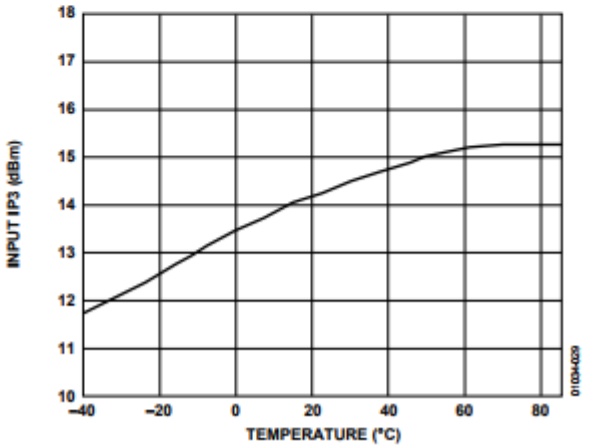

Figure 29. Input IP3 Performance Over Temperature; f_{IN} = 2400 MHz, f_{OUT} = 170 MHz

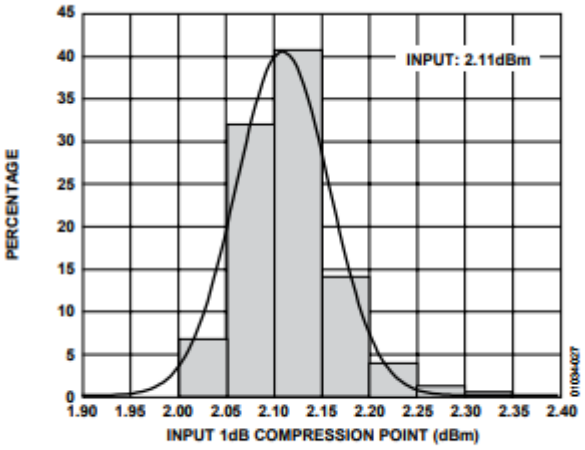

Figure 27. Input 1 dB Compression Point Histogram; f_{IN} = 2400 MHz, f_{OUT} = 170 MHz

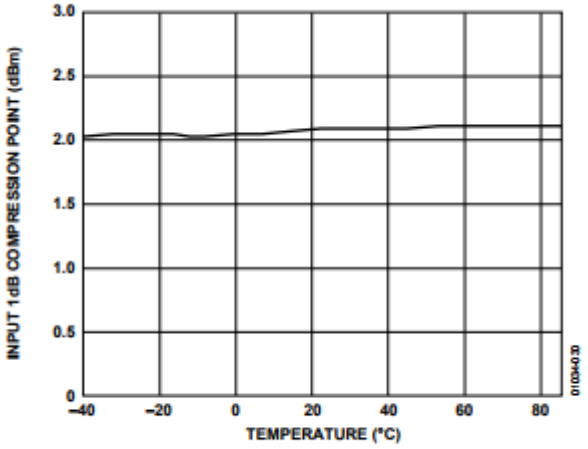

Figure 30. Input 1 dB Compression Point Performance Over Temperature; f_{IN} = 2400 MHz, f_{OUT} = 170 MHz

f_{IN} = 2400 MHz, f_{OUT} = 425 MHz, f_{LO} = 1975 MHz, see Figure 72, Table 6, and Table 8.

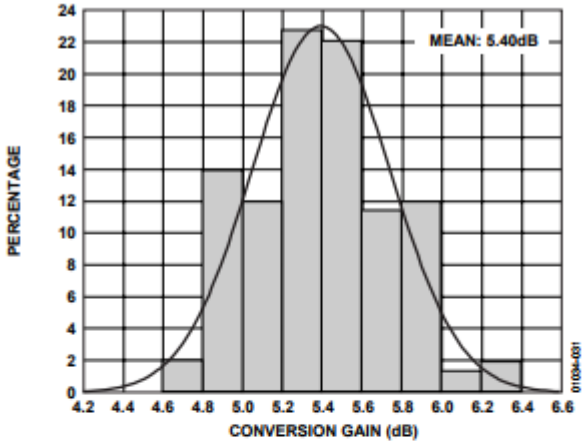

Figure 31. Gain Histogram; f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

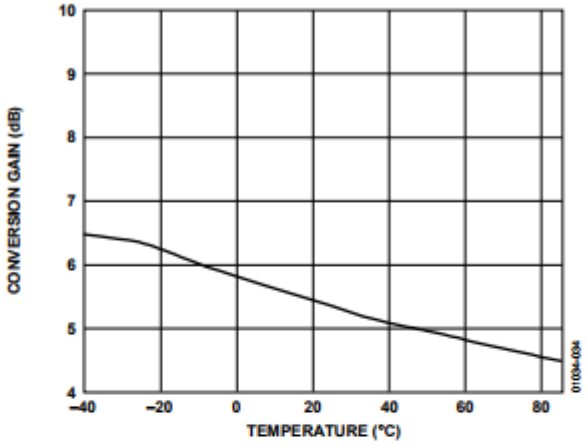

Figure 34. Gain Performance Over Temperature; f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

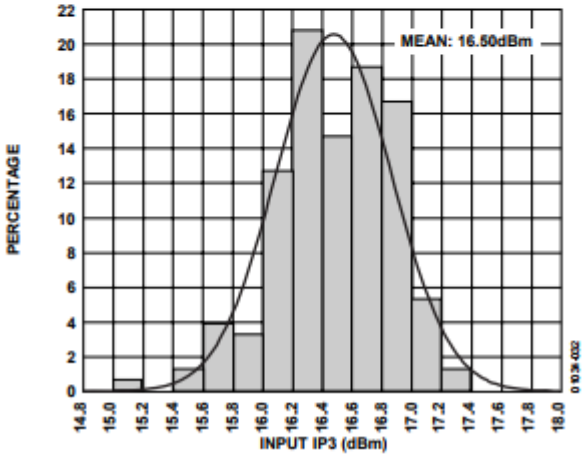

Figure 32. Input IP3 Histogram; f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

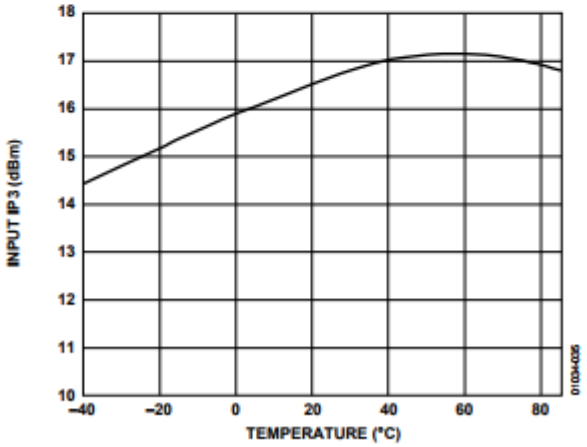

Figure 35. Input IP3 Performance Over Temperature; f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

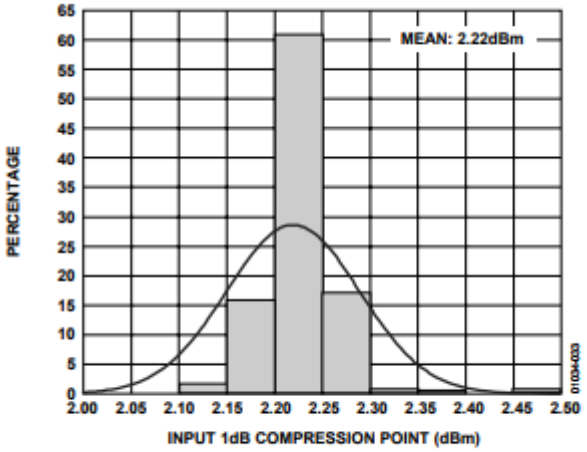

Figure 33. Input 1 dB Compression Point Histogram; f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

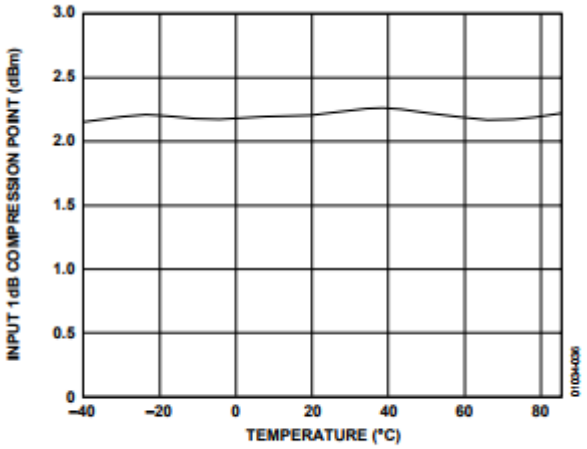

Figure 36. Input 1 dB Compression Point Performance Over Temperature; f_{IN} = 2400 MHz, f_{OUT} = 425 MHz

TRANSMIT CHARACTERISTICS

f_{IN} = 150 MHz, f_{OUT} = 900 MHz, f_{LO} = 750 MHz, see Figure 72, Table 6, and Table 7.

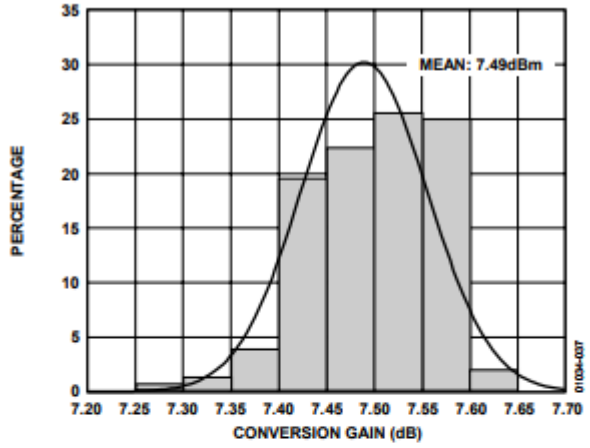

Figure 37. Gain Histogram; f_{IN} = 150 MHz, f_{OUT} = 900 MHz

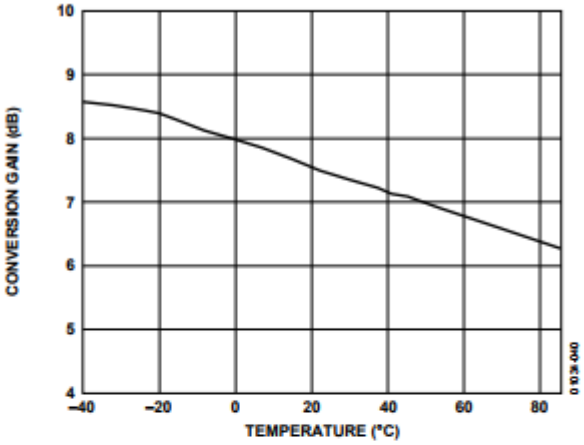

Figure 40. Gain Performance Over Temperature; f_{IN} = 150 MHz, f_{OUT} = 900 MHz

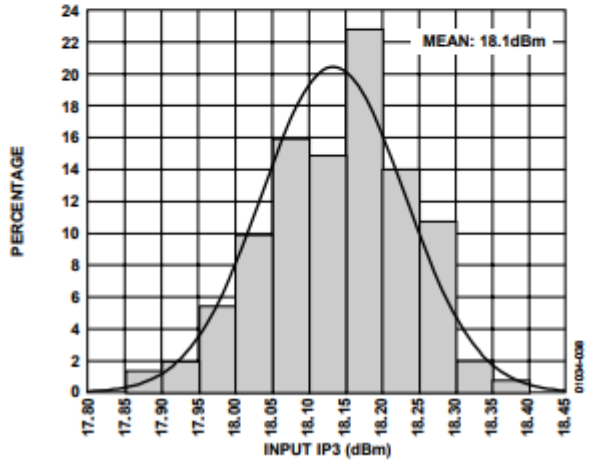

Figure 38. Input IP3 Histogram; f_{IN} = 150 MHz, f_{OUT} = 900 MHz

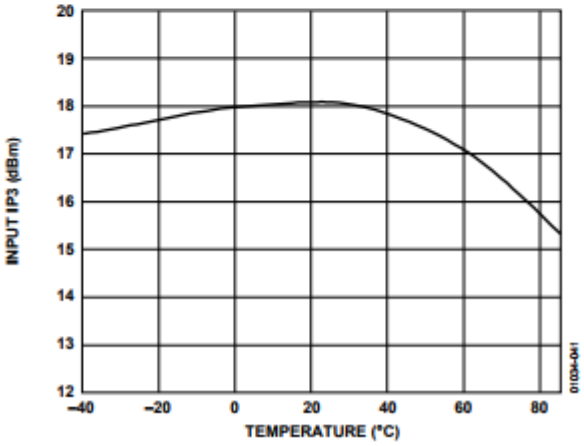

Figure 41. Input IP3 Performance Over Temperature; f_{IN} = 150 MHz, f_{OUT} = 900 MHz

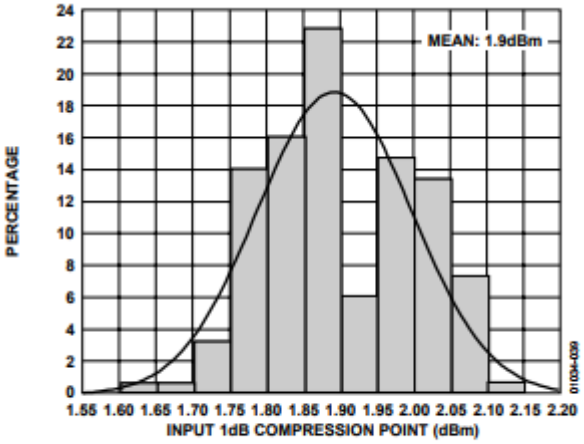

Figure 39. Input 1 dB Compression Point Histogram; f_{IN} = 150 MHz, f_{OUT} = 900 MHz

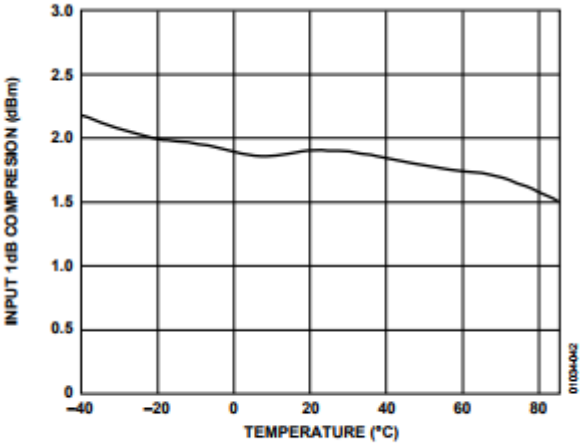

Figure 42. Input 1dB Compression Point Performance Over Temperature; f_{IN} = 150 MHz, f_{OUT} = 900 MHz

f_{IN} = 150 MHz, f_{OUT} = 1900 MHz, f_{LO} = 1750 MHz, see Figure 72, Table 6, and Table 7.

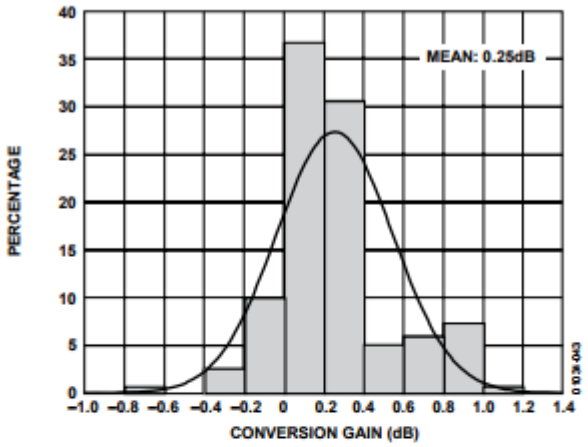

Figure 43. Gain Histogram; f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

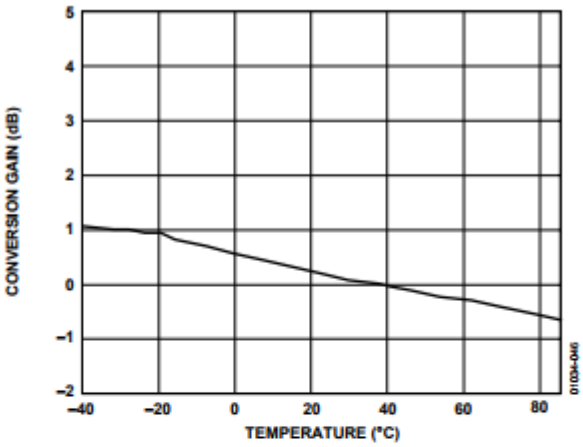

Figure 46. Gain Performance Over Temperature; f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

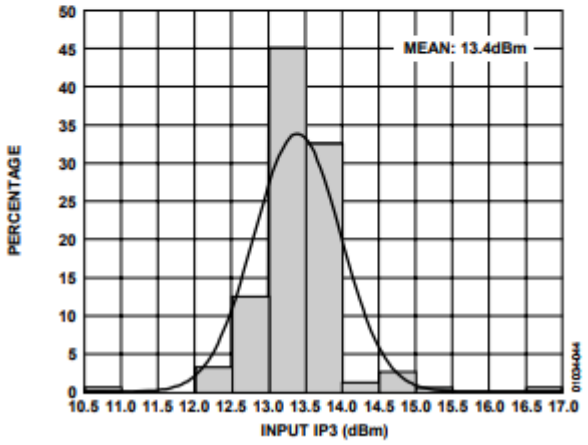

Figure 44. Input IP3 Histogram; f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

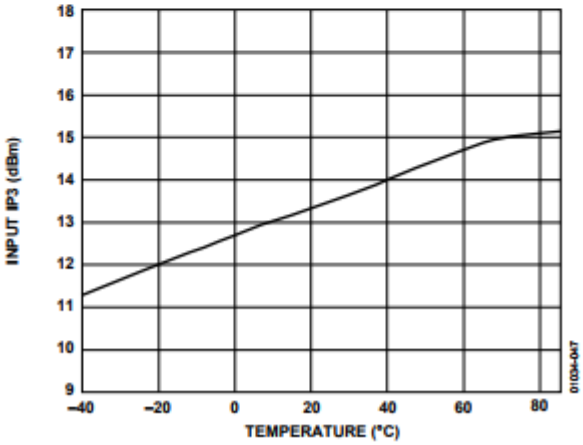

Figure 47. Input IP3 Performance Over Temperature; f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

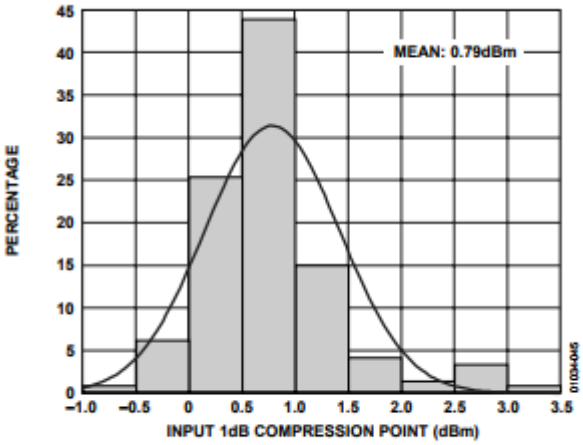

Figure 45. Input 1 dB Compression Point Histogram; f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

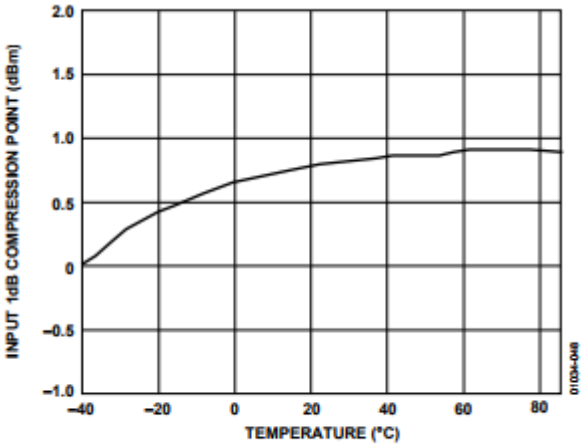

Figure 48. Input 1 dB Compression Point Performance Over Temperature; f_{IN} = 150 MHz, f_{OUT} = 1900 MHz

CIRCUIT DESCRIPTION

The AD8343 is a mixer intended for high-intercept applications. The signal paths are entirely differential and dc-coupled to permit high-performance operation over a broad range of frequencies; the block diagram (see Figure 1) shows the basic functional blocks. The bias cell provides a PTAT (proportional to absolute temperature) bias to the LO driver and core. The LO driver consists of a three-stage limiting differential amplifier that provides a very fast (almost square-wave) drive to the bases of the core transistors.

The AD8343 core utilizes a standard architecture where the signal inputs are directly applied to the emitters of the transistors in the cell (see Figure 49 and Figure 55). The bases are driven by the hard-limited LO signal that directs the transistors to steer the input currents into periodically alternating pairs of output terminals, thus providing the periodic polarity reversal that effectively multiplies the signal by a square wave of the LO frequency.

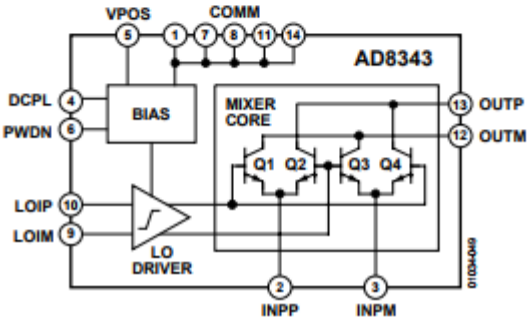

Figure 49. Topology

To illustrate this functionality, when LOIP is positive, Q1 and Q4 are turned on, and Q2 and Q3 are turned off. In this condition, Q1 connects I_{INPP} to OUTM and Q4 connects I_{INPM} to OUTP. When LOIP is negative, the roles of the transistors reverse, steering I_{INPP} to OUTP and I_{INPM} to OUTM. Isolation and gain are possible because, at any instant, the signal passes through a common-base transistor amplifier pair.

Multiplication is the essence of frequency mixing; an ideal multiplier would make an excellent mixer. The theory is expressed in the following trigonometric identity:

$$\sin(\omega_{sig}t) \times \sin(\omega_{LO}t) = \tfrac{1}{2}[\cos(\omega_{sig}t - \omega_{LO}t) - \cos(\omega_{sig}t + \omega_{LO}t)]$$

This states that the product of two sine-wave signals of different frequencies is a pair of sine waves at frequencies equal to the sum and difference of the two frequencies being multiplied.

Unfortunately, practical implementations of analog multipliers generally make poor mixers because of imperfect linearity and the added noise that invariably accompanies attempts to improve linearity. The best mixers to date are those that use the LO signal to periodically reverse the polarity of the input signal.

In this class of mixers, frequency conversion occurs as a result of multiplication of the signal by a square wave at the LO frequency. Because a square wave contains odd harmonics in addition to the fundamental, the signal is effectively multiplied by each frequency component of the LO. The output of the mixer therefore contains signals at $F_{LO} \pm F_{sig}$, $3\times F_{LO} \pm F_{sig}$, $5\times F_{LO} \pm F_{sig}$, $7\times F_{LO} \pm F_{sig}$, etc. The amplitude of the components arising from signal multiplication by LO harmonics falls off with increasing harmonic order because the amplitude of a square wave's harmonics falls off.

An example of this process is illustrated in Figure 50. The first pane of this figure shows an 800 MHz sinusoid intended to represent an input signal. The second pane contains a square wave representing an LO signal at 600 MHz which has been hard-limited by the internal LO driver. The third pane shows the time domain representation of the output waveform and the fourth pane shows the frequency domain representation. The two strongest lines in the spectrum are the sum and difference frequencies arising from multiplication of the signal by the LOs fundamental frequency. The weaker spectral lines are the result of the multiplication of the signal by various harmonics of the LO square wave.

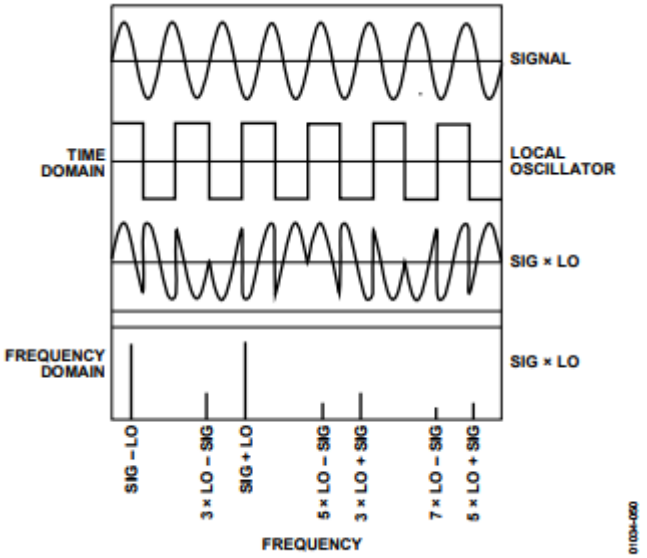

Figure 50. Signal Switching Characteristics of the AD8343

DC INTERFACES

BIASING AND DECOUPLING (VPOS, DCPL)

VPOS is the power supply connection for the internal bias circuit and the LO driver. Bypass this pin closely to GND with a capacitor in the range of 0.01 µF to 0.1 µF. The DCPL pin provides access to an internal bias node for noise bypassing purposes. Bypass this node to COMM with 0.1 µF.

POWER-DOWN INTERFACE (PWDN)

The AD8343 is active when the PWDN pin is held low; otherwise the device enters a low-power state as shown in Figure 51.

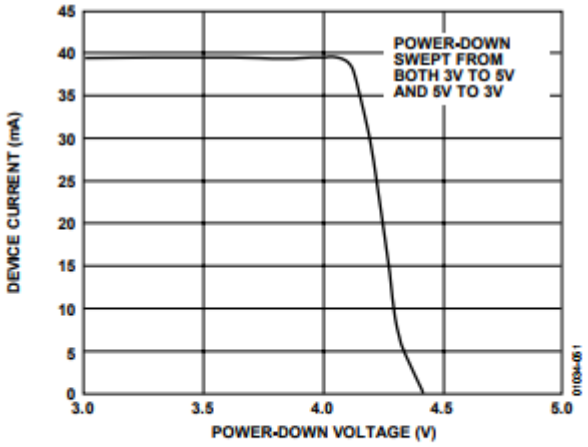

Figure 51. Device Current vs. PWDN Voltage

To assure full power-down, the PWDN voltage must be within 0.5 V of the supply voltage at VPOS. Normal operation requires that the PWDN pin be taken at least 1.5 V below the supply voltage. The PWDN pin sources about 160 µA when pulled to GND (see the Pin Configuration and Function Descriptions section). It is not advised to leave the pin floating when the device is disabled; a resistive pull-up to VPOS is the minimum suggestion.

The AD8343 requires about 2.2 µs to turn off when PWDN is asserted; turn-on time is about 500 ns. Figure 52 and Figure 53 show typical characteristics (they vary with bypass component values). Figure 54 shows the test configuration used to acquire these waveforms.

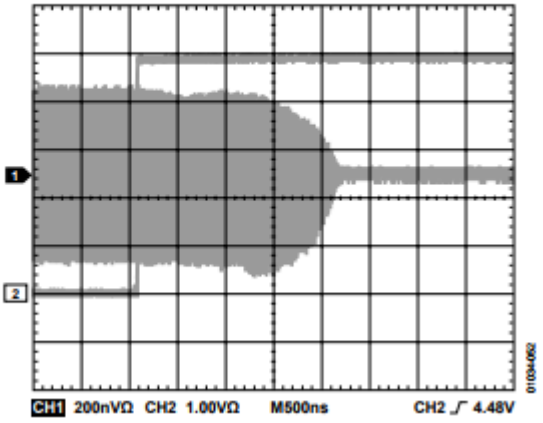

Figure 52. PWDN Response Time Device On to Off

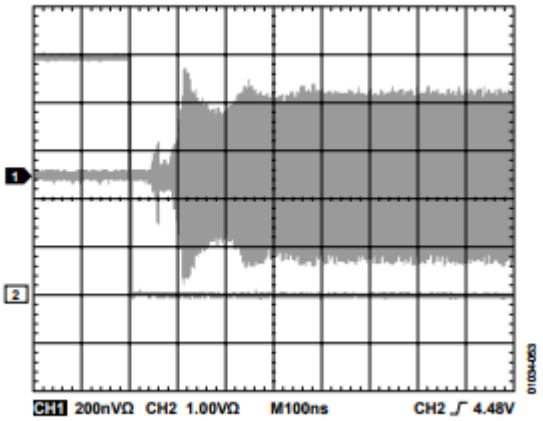

Figure 53. PWDN Response Time Device Off to On

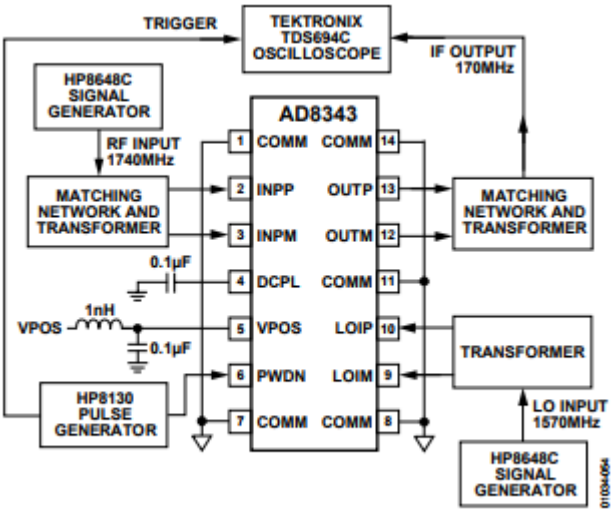

Figure 54. PWDN Response Time Test Schematic

AC INTERFACES

Because of the AD8343's wideband design, there are several points to consider in its ac implementation; the basic ac signal connection diagram shown in Figure 55 summarizes these points. The input signal undergoes a single-ended to differential conversion and is then reactively matched to the impedance presented by the emitters of the core. The matching network also provides bias currents to these emitters. Similarly, the LO input undergoes a single-ended-to-differential transformation before it is applied to the 50 Ω differential LO port. The differential output signal currents appear at open-collectors and are reactively matched and converted to a single-ended signal.

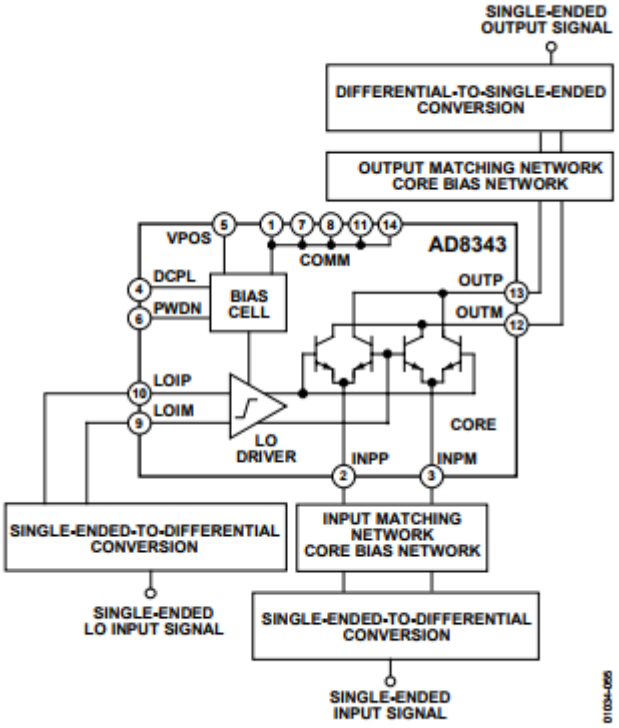

Figure 55. Basic AC Signal Connection Diagram

INPUT INTERFACE (INPP AND INPM)

SINGLE-ENDED-TO-DIFFERENTIAL CONVERSION

The AD8343 is designed to accept differential input signals for best performance. While a single-ended input can be applied, the signal capacity is reduced by 6 dB. Furthermore, there is no cancellation of even-order distortion arising from the nonlinear input impedances, so the effective signal handling capacity is reduced even further in distortion-sensitive situations. That is, the intermodulation intercepts are degraded.

For these reasons, it is strongly recommended that differ ential signals be presented to the AD8343's input. In addition to commercially available baluns, there are various discrete and printed circuit networks that can produce the required balanced waveforms and impedance match. These alternate circuits can be employed to possibly reduce the component cost of the mixer and/or improve performance.

Baluns implemented in transmission line form (also known as common-mode chokes) are useful up to frequencies of around 1 GHz to 2 GHz, but are often excessively lossy at the higher frequencies that the AD8343 can handle. M/A-COM manufac tures these baluns and Murata produces a true surface-mount balun. Coilcraft* and Toko are also manufacturers of RF baluns.

INPUT MATCHING CONSIDERATIONS

The design of the input matching network must be undertaken with two goals in mind: matching the source impedance to the input impedance of the AD8343 and providing a dc bias current path for the bias setting resistors.

The maximum power transfer into the device occurs when there is a conjugate impedance match between the signal source and the input of the AD8343. This match is achieved with the differential equivalent of the classic L network, as illustrated in Figure 56. The figure gives two examples of the transformation from a single-ended L network to its differential counterpart. The design of L matching networks is adequately covered in texts on RF amplifier design (for example, *Microwave Transistor Amplifiers* by Guillermo Gonzalez).

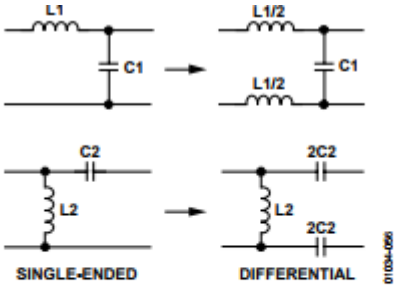

Figure 56. Single-Ended-to-Differential Transformation

Figure 57 shows the differential input impedance of the AD8343 at the pins of the device. The two measurements shown in the figure are for two different core currents set by Resistor R3 and Resistor R4; the real value impedance shift is caused by the change in Transistor r_e due to the change in current. The standard S parameter files are available through Analog Devices.

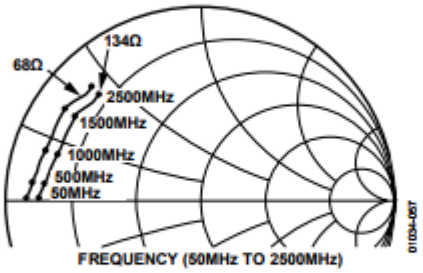

Figure 57. Input Differential Impedance (INPP, INPM) for Two Values of R3 and R4

Figure 57 provides a reasonable starting point for the design of the network. However, the particular board traces and pads transform the input impedance at frequencies in excess of about 500 MHz. For this reason, it is best to make a differential input impedance measurement at the board location where the matching network is installed, as a starting point for designing an accurate matching network.

Differential impedance measurement is made relatively easy using a technique presented in an article by Lutz Konstroffer in *RF Design*, Vol. 22, January 1999, Page 24, 28; entitled "Finding the Reflection Coefficient of a Differential One-Port Device." This article presents a mathematical formula for converting from a two-port single ended measurement to differential impedance. A full two-port measurement is performed using a vector network analyzer with Port 1 and Port 2 connected to the two differential inputs of the device at the desired measurement plane. The two-port measurement results are then processed with Konstroffer's formula. This formula is straightforward and can be implemented through most RF design packages that can read and analyze network analyzer data. The Konstroffer formula is:

$$\Gamma s = \frac{(2\times S11 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22 - 2\times S12)}{(2 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22)}$$

This measurement can also be made using two ports of a 4-port vector network analyzer. This instrument, and accompanying software, is capable of directly producing differential measurements.

At low frequencies and I_O = 16 mA, the differential input impedance seen at ports INPP and INPM of the AD8343 is low (~5 Ω in series with parasitic inductances that total about 3 nH). Because of this low value of impedance, it is beneficial to choose a transformer-type balun that can also perform all or part of the real value impedance transformation. The turns ratio of the transformer removes some of the matching burden from the differential L-network and should help lead to wider

bandwidth matches. At frequencies above 1 GHz, the real part of the input impedance rises markedly and it becomes more attractive to use a 1:1 balun and rely on the L network for the entire impedance transformation.

In order to obtain the lowest distortion, the inputs of the AD8343 are driven through external ballast resistors. At low frequencies (up to perhaps 200 MHz), about 5 Ω per side is appropriate; above about 400 MHz, 10 Ω per side is better. The specified RF performance values for the AD8343 apply with these ballast resistors in use. These resistors improve linearity because their linear ac voltage drop partially swamps the nonlinear voltage swing occurring on the emitters.

In cases where the use of a lossy balun is unavoidable, it can be worthwhile to perform simultaneous matching on both the input and output sides of the balun. The idea is to independently characterize the balun as a two-port device and then arrange a simultaneous conjugate match for it. Unfortunately, there seems to be no good way to determine the benefit this approach offers in any particular case; it remains necessary to characterize the balun and then design and simulate appropriate matching networks to make an optimal decision. One indication that such effort is worthwhile is the discovery that the adjustment of a post-balun-only matching network for best gain differs appreciably from that which produces best return loss at the baluns input. A better tactic is to try a different approach for the balun, either purchasing a different balun or designing a discrete network, for lower loss.

For more information on performing the input match, see the section entitled A Step-by-Step Approach to Impedance Matching.

INPUT BIASING CONSIDERATIONS

The mixer core bias current of the AD8343 is adjustable from less than 5 mA to a safe maximum of 20 mA. It is important to note that the reliability of the AD8343 can be compromised for core currents set to higher than 20 mA. The AD8343 is tested to ensure that a value of 68.1 Ω ±1% ensures safe operation.

Higher operating currents reduce distortion and affect gain, noise figure, and input impedance (Figure 58 and Figure 59). As the quiescent current is increased by a factor of N, the real part of the input impedance decreases by N. Assuming that a match is maintained, the signal current increases by √N, but the signal voltage decreases by √N, exercising a smaller portion of the nonlinear V–I characteristic of the common base connected mixer core transistors and results in lower distortion.

At low frequencies where the magnitude of the complex input impedance is much smaller than the bias resistor values, adequate biasing can be achieved simply by connecting a resistor from each input to GND. The input terminals are internally biased at 1.2 V dc (nominal), so each resistor has a resistance value calculated as $R_{BIAS} = 1.2/I_{BIAS}$. The resistor values should be well matched in order to maintain full LO to output isolation; 1% tolerance resistors are recommended.

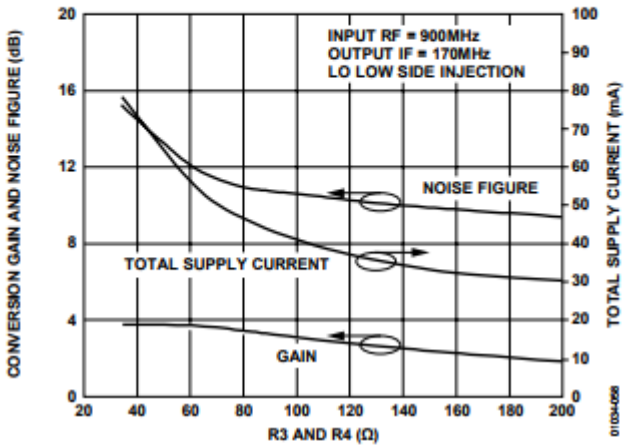

Figure 58. Effect of R3 and R4 Value on Gain and Noise Figure

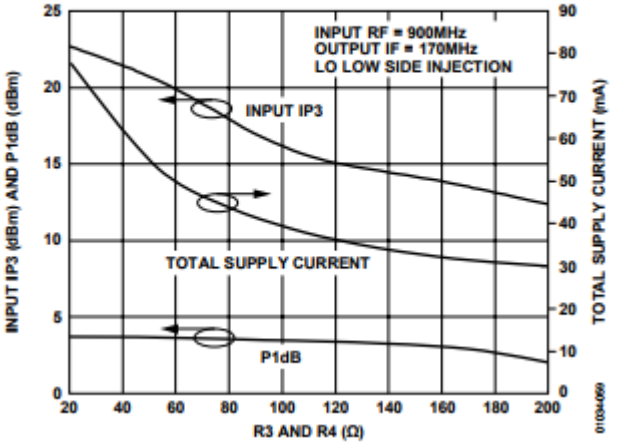

Figure 59. Effect of R3 and R4 Value on Input IP3 and Gain Compression

At higher frequencies where the input impedance of the AD8343 rises, it is beneficial to insert an inductor in series between each bias resistor and the corresponding input pin in order to minimize signal shunting (Figure 72). Practical considerations limit the inductive reactance to a few hundred ohms. The best overal choice of inductor is the value that places the self-resonant frequency at about the upper end of the desired input frequency range. Note that there is an RF stability concern that argues in favor of erring on the side of too small an inductor value; see the Input and Output Stability Considerations section. The Murata LQW1608A series of inductors (0603 SMT package) offers values up to 56 nH before the self-resonant frequency falls below 2.4 GHz.

For optimal LO-to-output isolation, it is important not to connect the dc nodes of the emitter bias inductors together in an attempt to share a single bias resistor. Doing so causes isolation degradation arising from V_{BE} mismatches of the transistors in the core.

OUTPUT INTERFACE (OUTP, OUTM)

The output of the AD8343 comprises a balanced pair of open collector outputs. These should be biased to about the same voltage as is connected to VPOS. Connecting them to an appreciably higher voltage is likely to result in conduction of the ESD protection network on signal peaks, causing high distortion levels. On the other hand, setting the dc level of the outputs too low is also likely to result in poor device linearity due to collector-base capacitance modulation or saturation of the mixer core transistors.

OUTPUT MATCHING CONSIDERATIONS

The AD8343 requires a differential load for much the same reasons that the input needs a differential source to achieve optimal device performance. In addition, a differential load provides the best LO to output isolation and the best input to output isolation.

At low output frequencies, it is usually not appropriate to arrange a conjugate match between the device output and the load, even though doing so maximizes the small signal conversion gain. This is because the output impedance at low frequencies is quite high (a high resistance in parallel with a small capacitance). See Figure 60 for a plot of the differential output impedance measured at the device pins. This data is available in standard file format at the Analog Devices website (http://www.analog.com); search for AD8343, then click on *AD8343 S-Parameters*. If a matching high impedance load is used, sufficient output voltage swing occurs to cause output clipping even at relatively low input levels, constituting a loss

clipping even at relatively low input levels, constituting a loss of dynamic range. The linear range of voltage swing at each output pin is about ±1 V from the supply voltage VPOS. A good compromise is to provide a load impedance of about 200 Ω to 500 Ω between the output pins at the desired output frequency (based on 15 mA to 20 mA bias current at each input). At output frequencies below 500 MHz, more output power can be obtained before the onset of gross clipping by using a lower load impedance; however, both gain and low order distortion performance can be degraded.

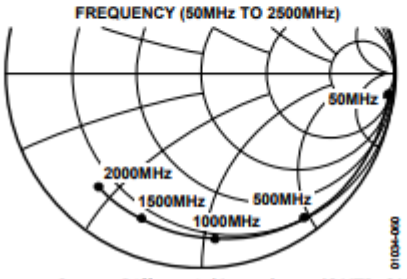

Figure 60. Output Differential Impedance (OUTP, OUTM)

The output load impedance must also be kept reasonably low at the image frequency to avoid developing appreciable extra voltage swing, which can reduce dynamic range.

If maintaining a good output return loss is not required, a 4:1 to 8:1 (impedance) flux-coupled transformer can be used to present a suitable load to the device and to provide collector bias via a center tap as shown in Figure 69. At all but the lowest output frequencies, it becomes desirable to tune out the output capacitance of the AD8343 by connecting an inductor between the output pins. On the other hand, when a good output return loss is desired, the output can be resistively loaded with a shunt resistance between the output pins in order to set the real value of output impedance. With selection of both the transformer's impedance ratio and the shunting resistance as required, the desired total load (~500 Ω) is achieved while optimizing both signal transfer and output return loss.

At higher output frequencies, the output conductance of the device becomes higher (see Figure 60), with the consequence that above about 900 MHz, it does become appropriate to perform a conjugate match between the load and the AD8343s output. The device's own output admittance becomes sufficient to remove the threat of clipping from excessive voltage swing. Just as for the input, it is best to perform differential output impedance measurements on the board layout to effectively develop a good matching network.

OUTPUT BIASING CONSIDERATIONS

OUTPUT BIASING CONSIDERATIONS

When the output single-ended-to-differential conversion takes the form of a transformer whose primary winding is center tapped, simply apply VPOS to the tap, preferably through a ferrite bead in series with the tap in order to avoid a common mode instability problem (see the Input and Output Stability Considerations section). See Figure 69 for an example of this network. The collector dc bias voltage must be nominally equal to the supply voltage applied to Pin 5 (VPOS).

If a 1:1 transmission line balun is used for the output, it is necessary to bring in collector bias through separate inductors. These inductors are chosen to obtain a high impedance over the RF output frequency range of interest. See Figure 70 for an example of this network.

INPUT AND OUTPUT STABILITY CONSIDERATIONS

The differential configuration of the input and output ports of the AD8343 raises the need to consider both differential and common-mode RF stability of the device. Throughout the following stability discussion, common mode is used to refer to a signal that is referenced to ground. The equivalent common-mode impedance is the value of impedance seen from the node under discussion to ground. The book, *Microwave Transistor Amplifiers* by Guillermo Gonzalez, also has an excellent section covering stability of amplifiers.

The AD8343 is unconditionally stable for any differential impedance, so device stability need not be considered with respect to the differential terminations. However, the device is potentially unstable (k factor is less than one) for some common-mode impedances. Figure 61 and Figure 62 plot the input and output common-mode stability regions, respectively. Figure 63 shows the test equipment configuration to measure these stability circles.

The plotted stability circles in Figure 62 indicate that the guiding principle for preventing stability problems due to common-mode output loading is to avoid high-Q common-mode inductive loading. This stability concern is of particular importance when the output is taken from the device with a center-tapped transformer. The common-mode inductance to the center tap arises from imperfect coupling between the halves of the primary winding and produces an unstable common-mode loading condition. Fortunately, a simple solution is to insert a ferrite bead in series with the center tap, then provide effective RF bypassing on the power supply side of the bead. The bead develops substantial impedance (tens of ohms) by the time a frequency of about 200 MHz is reached. The Murata BLM21P300S is a possible choice for many applications.

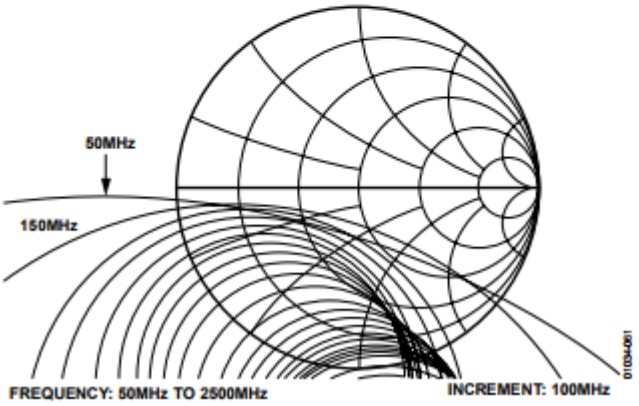

Figure 61. Common-Mode Input Stability Circles

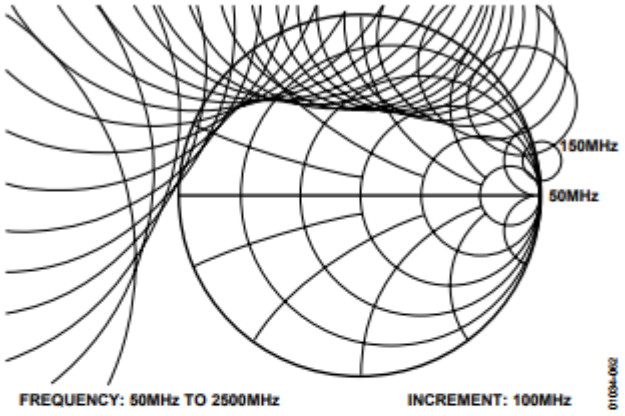

Figure 62. Common-Mode Output Stability Circles

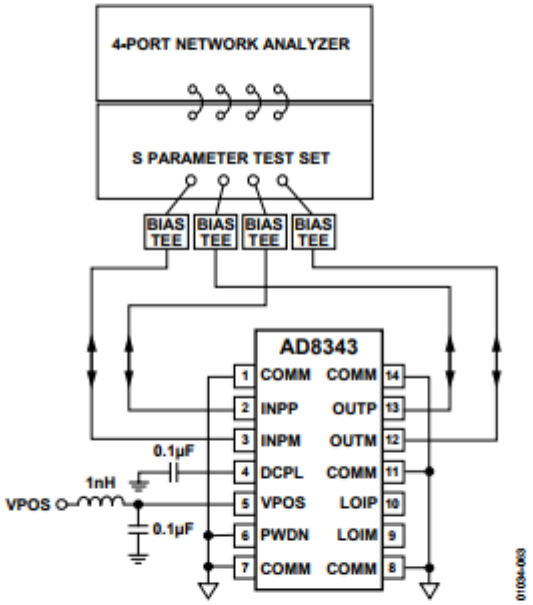

Figure 63. Impedance and Stability Circle Test Schematic

In cases where a transmission line balun is used at the output, the solution deserves a bit more exploration. After the differential impedance matching network is designed, it is possible to measure or simulate the common-mode impedance seen by the device. This impedance is plotted against the stability circles to ensure stable operation. An alternate topology for the matching network is required if the proposed network produces an unacceptable common-mode impedance.

For the device input, capacitive common-mode loading tends to produce an unstable circuit, particularly at low frequencies (see Figure 61). Fortunately, either type of single-ended-to-differential conversion (transmission line balun or flux-coupled transformer) tends to produce inductive loading, although some matching network topologies and/or component values circumvent this desirable behavior. In general, a simulation of the common-mode termination seen by the AD8343's input port is plotted against the input stability circles to check stability. This is especially recommended if the single-ended-to-differential conversion is done with a discrete component circuit.

LOCAL OSCILLATOR INPUT INTERFACE (LOIP, LOIM)

The LO terminals of the AD8343 are internally biased; connections to these terminals should include dc blocks, except as noted below in the DC Coupling the LO section.

The differential LO input return loss (with a 50 Ω differential input impedance) is presented in Figure 64. As shown, this port has a typical differential return loss of better than 9.5 dB (2:1 V SWR). If better return loss is desired for this port, differential matching techniques can also be applied.

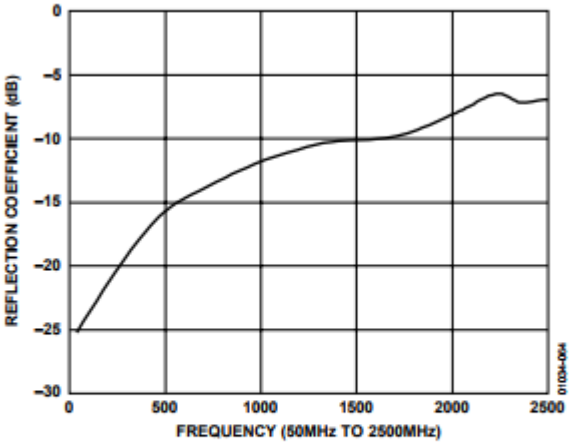

Figure 64. LO Input Differential Reflection Coefficient

At low LO frequencies, it is reasonable to drive the AD8343 with a single-ended LO, connecting the undriven LO pin to GND through a dc block. This results in an LO input impedance closer to 25 Ω at low frequencies, which should be factored into the design. At higher LO frequencies, differential drive is strongly recommended.

The suggested minimum LO power level is about –12 dBm. This can be seen in Figure 65.

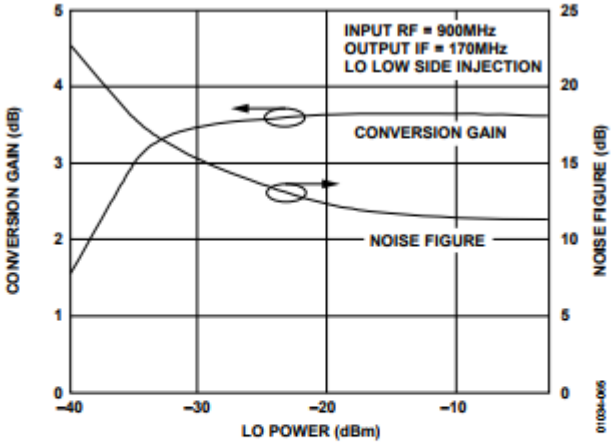

Figure 65. Gain and Noise Figure vs. LO Input Power

DC COUPLING THE LO

The AD8343's LO limiting amplifier chain is internally dc-coupled. In some applications or experimental situations, it is useful to exploit this property. Following is the recommended way to do so.

The LO pins are internally biased at about 360 mV with respect to COMM. Driving the LO to either extreme requires injecting several hundred microamps into one LO pin and extracting about the same amount of current from the other. The incremental impedance at each pin is about 25 Ω, so the voltage level on each pin is disturbed very little by the application of external currents in that range.

Figure 66 illustrates how to drive the LO port with continuous dc and also from standard ECL powered by –5.2 V.

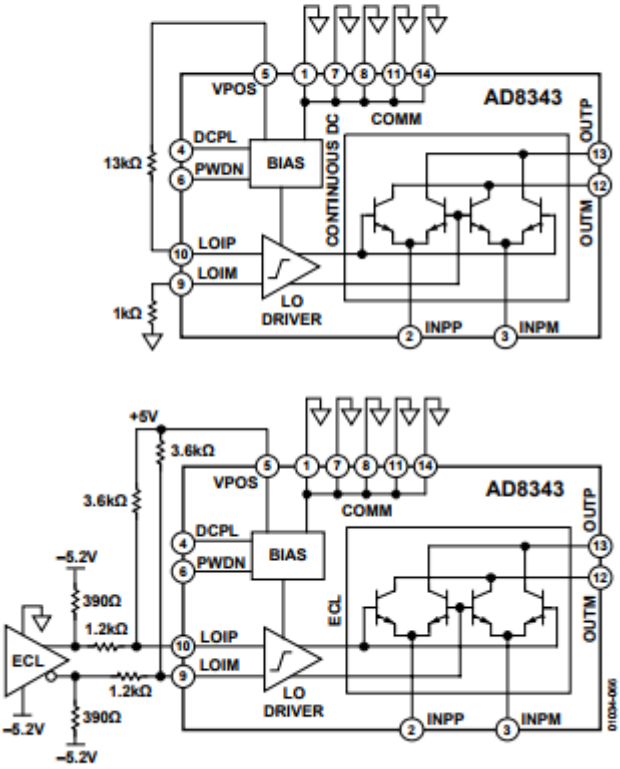

Figure 66. DC Interfaces to the LO Port

A STEP-BY-STEP APPROACH TO IMPEDANCE MATCHING

The following discussion addresses, in detail, the matter of establishing a differential impedance match to the AD8343. This section specifically deals with the input match, and the use of Side A of the evaluation board (Figure 71). An analogous procedure is used to establish a match to the output if desired.

Circuit Setup

The AD8343 must be powered up, driven with LO; its outputs are terminated in a manner that avoids the common-mode stability problem, as discussed in the Input and Output Stability Considerations section. A convenient way to deal with the output termination is to place ferrite chokes at L3A and L4A and omit the output matching components altogether.

It is also important to establish the means of providing bias currents to the input pins because this network can have unexpected loading effects and inhibit matching progress.

Establish Target Impedance

This step is necessary when the single-ended-to-differential network (input balun) does not produce a 50 Ω output impedance. In order to provide for maximum power transfer, the input impedance of the matching network, loaded with the AD8343 input impedance (including ballast resistors), is the conjugate of the output impedance of the single-ended-to-differential network. This step is of particular importance when utilizing transmission line baluns because the differential output impedance of the input balun can differ significantly from what is expected. Therefore, it is a good idea to make a separate measurement of this impedance at the desired operating frequency before proceeding with the matching of the AD8343.

The idea is to make a differential measurement at the output of the balun, with the single-ended port of the balun terminated in 50 Ω. Again, there are two methods available for making this measurement: use of the ATN multiport network analyzer to measure the differential impedance directly, or use of a standard two-port network analyzer and Konstroffer's transformation equation.

In order to utilize a standard two-port analyzer, connect the two ports of the calibrated vector network analyzer (VNA) to the balanced output pins of the balun, measure the two-port S parameters, then use Konstroffer's formula to convert the two-port parameters to one-port differential Γ:

$$\Gamma s = \frac{(2 \times S11 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22 - 2 \times S12)}{(2 - S21)(1 - S22 - S12) + (1 - S11 - S21)(1 + S22)}$$

Measure AD8343 Differential Impedance at Location of First Matching Component

Once the target impedance is established, the next step in matching to the AD8343 is to measure the differential impedance at the location of the first matching component. The A side of the evaluation board is designed to facilitate doing so.

Before doing the board measurements, it is necessary to perform a full two-port calibration of the VNA at the ends of the cables that are used to connect to the board's input connectors, using the SOLT (Short, Open, Load, Thru) method or equivalent. It is a good idea to set the VNAs sweep span to a few hundred megahertz or more for this work because it is often useful to see what the circuit is doing over a large range of frequencies, not just at the intended operating frequency. This is particularly useful for detecting stability problems.

After the calibration is complete, connect Network Analyzer Port 1 and Network Analyzer Port 2 to the differential inputs of the AD8343 Evaluation Board.

On the AD8343 evaluation board, it is necessary to temporarily install jumpers at Z1A and Z3A if Z4A is the desired component location. 0 Ω resistors or capacitors of sufficient value to exhibit negligible reactance work nicely for this purpose.

Next, extend the reference plane to the location of your first matching component. This is accomplished by solidly shorting both pads at the component location to GND Power to the board must be off for this operation. Adjust the VNA reference plane extensions to make the entire trace collapse to a point (or best approximation thereof near the desired frequency) at the zero impedance point of the Smith Chart. Do this for each port. A reasonable way to provide a good RF short is to solder a piece of thin copper or brass sheet on edge across the pads to the nearby GND pads.

Now, remove the short, apply power to the board, and take readings. Look at both S11 and S22 to verify that they remain inside the unit circle of the Smith Chart over the whole frequency range being swept. If they fail to do so, this is a sign that the device is unstable (perhaps due to an inappropriate common-mode load) or that the network analyzer calibration is wrong. Either way, the problem must be addressed before proceeding further.

Assuming that the values look reasonable, use Konstroffer's formula to convert to differential Γ.

Design the Matching Network

Perform a trial design of a matching network utilizing standard impedance matching techniques. The network can be designed using single-ended network values, and then converted to differential form as illustrated in Figure 56. Figure 67 shows a theoretical design of a Series C/Shunt C L-network applied between 50 Ω and a typical load at 1.8 GHz.

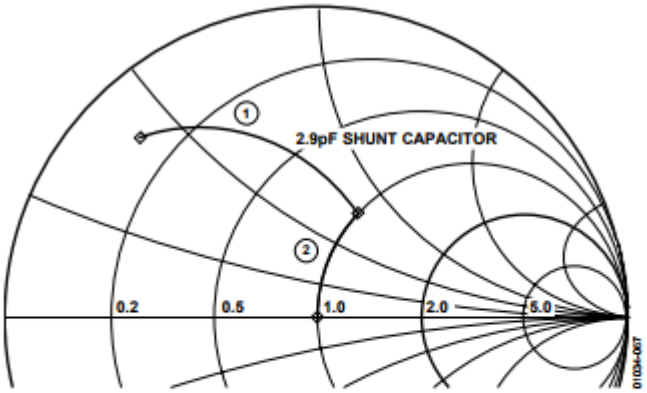

Figure 67. Theoretical Design of Matching Network

This theoretical design is important because it establishes the basic topology and the initial matching value for the network. The theoretical value of 2.9 pF for the initial matching component is not available in standard capacitor values, so a 3.0 pF is placed in the first shunt-matching location. This value can prove to be too large, causing an overshoot of the 50 Ω real impedance circle, or too small, causing the opposite effect. Always keep in mind that this is a measure of differential impedance. The value of the capacitor must be modified to achieve the desired 50 Ω real impedance.

However, it occasionally happens that the inserted shunt capacitor moves the impedance in completely unexpected and undesired ways. This is almost always an indication that the reference plane was improperly extended for the measurement. Readjust the reference planes and attempt the shunt capacitor match with another calculated value.

When a differential impedance of 50 Ω (real part) is achieved, the board must be powered down and then another short is placed on the board in preparation for resetting the port extensions to a new reference plane location. Place this short where the next series components are expected to be added, and it is important that both Port 1 and Port 2 be extended to this point on the board.

Another differential measurement must be taken at this point to establish the starting impedance value for the next matching component. Note that if 50 Ω PCB traces of finite length are used to connect pads, the impedance experiences an angular rotation to another location on the Smith Chart as indicated in Figure 68.

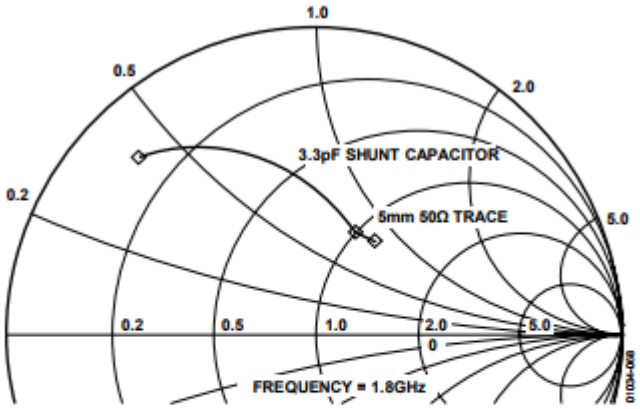

Figure 68. Effect of 50 Ω PCB Trace on 50 Ω Real Impedance Load

With the reference plane extended to the location of the series matching components, it is now necessary to readjust the shunt capacitance value to achieve the desired 50 Ω real impedance. However, this rotation is not very noticeable if the board traces are fairly short or the application frequency is low.

As before, calculate the series capacitance value required to move in the direction shown as step two in Figure 67. Choose the nearest standard component remembering to perform the differential conversion, and install on the board. Again, if any unexpected impedance transformations occur the reference planes were probably extended incorrectly making it necessary to readjust these planes.

This value of series capacitance adjusts to obtain the desired value of differential impedance.

These steps apply to any of the previously discussed matching topologies suitable for the AD8343. Also, if a target impedance other than 50 Ω is required, simply calculate and adjust the components to obtain the desired load impedance.

If the matching network topology requires a differential shunt inductor between the inputs, it is necessary to place a series blocking capacitor of low reactance in series with the inductor to avoid creating a low resistance dc path between the input terminals of the AD8343. Failure to heed this warning results in very poor LO-output isolation.

Transfer the Matching Network to the Final Design

On the B side of the AD8343 evaluation board, install the matching network and the input balun. Install the same output network as used for the work on the A side, then power up the board and measure the input return loss at the RF input connector on the board. Strictly speaking, the above procedure (if carried out accurately) for matching the AD8343 obtains the best conversion gain. This differs materially from the condition that results in best return loss at the board's input if the balun is lossy.