TPS736xx Cap-Free, NMOS, 400-mA Low-Dropout Regulator with Reverse Current Protection

1 Features

- Stable with No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range of 1.7 V to 5.5 V
- Ultra-Low Dropout Voltage: 75 mV typ
- Excellent Load Transient Response—with or without Optional Output Capacitor
- New NMOS Topology Delivers Low Reverse Leakage Current
- Low Noise: 30 μV_{RMS} typ (10 Hz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy Over Line, Load, and Temperature
- Less Than 1 µA max I_Q in Shutdown Mode
- Thermal Shutdown and Specified Min/Max Current Limit Protection
- Available in Multiple Output Voltage Versions
  - Fixed Outputs of 1.20 V to 5.0 V
  - Adjustable Output from 1.20 V to 5.5 V
  - Custom Outputs Available

2 Applications

- Portable/Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry such as VCOs
- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

3 Description

The TPS736xx family of low-dropout (LDO) linear voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. It also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

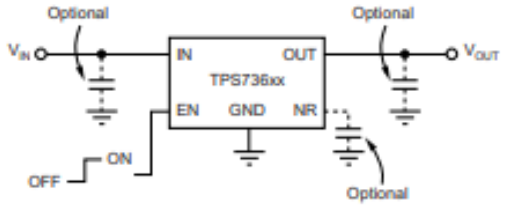
The TPS736xx uses an advanced BiCMOS process to yield high precision while delivering very low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1-µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS736xx	SOT-23 (5)	2.90 mm x 1.60 mm
	SOT-223 (6)	6.50 mm x 3.50 mm
	VSON (8)	3.00 mm x 3.00 mm

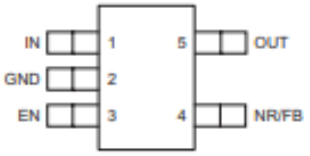
(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit for Fixed-Voltage Versions

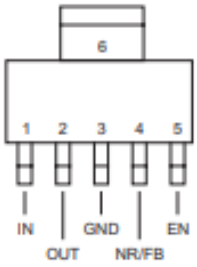


5 Pin Configuration and Functions

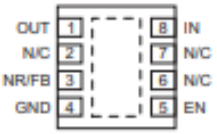
DBV Package
5-Pin SOT23
(Top View)



DCQ Package
6-Pin SOT223
(Top View)



DRB Package
8-Pin VSON
(Top View)



Pin Functions

PIN				I/O	DESCRIPTION
NAME	NO.				
	SOT23	SOT223	VSON		
IN	1	1	8	I	Input supply
GND	2	3, 6	4, Pad	—	Ground
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. Refer to the *Shutdown* section for more details. EN can be connected to IN if not used.
NR	4	4	3	—	Fixed-voltage versions only. Connecting an external capacitor to this noise reduction pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
FB	4	4	3	I	Adjustable-voltage version only. This pin is the input to the control loop error amplifier, and sets the output voltage of the device.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.

6.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage	V_{IN}	–0.3	+6.0	V
	V_{EN}	–0.3	+6.0	V
	V_{OUT}	–0.3	+5.5	V
	V_{NR}, V_{FB}	–0.3	+6.0	V
Peak output current	I_{OUT}	Internally limited		
Output short-circuit duration		Indefinite		
Continuous total power dissipation	P_{DISS}	See *Thermal Information*		
T_J	Junction temperature range	–55	150	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. *Electrical Characteristics* Exposure to absolute maximum rated conditions for extended periods may affect device reliability

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage range	1.7		5.5	V
I_{OUT}	Output current	0		500	mA
T_J	Operating junction temperature	–40		125	°C

6.4 Thermal Information

THERMAL METRIC[1][2]		TPS736[3]			UNIT
		DRB/SON	DCQ/SOT223	DBV/SOT23	
		8 PINS	6 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance[4]	52.8	118.7	221.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance[5]	60.4	64.9	74.9	
$R_{\theta JB}$	Junction-to-board thermal resistance[6]	28.4	65.0	51.9	
ψ_{JT}	Junction-to-top characterization parameter[7]	2.1	14.0	2.8	
ψ_{JB}	Junction-to-board characterization parameter[8]	28.6	63.8	51.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance[9]	12.0	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the *TI PCB Thermal Calculator*.
(3) Thermal data for the DRB, DCQ, and DRV packages are derived by thermal simulations based on JEDEC-standard methodology as specified in the JESD51 series. The following assumptions are used in the simulations:
  (a) i. DRB: The exposed pad is connected to the PCB ground layer through a 2x2 thermal via array.
  ii. DCQ: The exposed pad is connected to the PCB ground layer through a 3x2 thermal via array.
  iii. DBV: There is no exposed pad with the DBV package.
  (b) i. DRB: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  ii. DCQ: Each of top and bottom copper layers has a dedicated pattern for 20% copper coverage.
  iii. DBV: The top and bottom copper layers are assumed to have a 20% thermal conductivity of copper representing a 20% copper coverage.
  (c) These data were generated with only a single device at the center of a JEDEC high-K (2s2p) board with 3in × 3in copper area. To understand the effects of the copper area on thermal performance, see the *Power Dissipation* section of this data sheet.
(4) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(5) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the top of the package. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(6) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(7) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(8) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data to obtain θ_{JA} using a procedure described in JESD51-2a (sections 6 and 7).
(9) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V[1], I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range[1][2]			1.7		5.5	V
V_{FB}	Internal reference (TPS73601)		T_J = 25°C	1.198	1.20	1.210	V
V_{OUT}	Output voltage range (TPS73601)[3]			V_{FB}		5.5 – V_{DO}	V
	Accuracy[1][4]	Nominal	T_J = 25°C	–0.5		+0.5	
		over V_{IN}, I_{OUT}, and T	V_{OUT} + 0.5 V ≤ V_{IN} ≤ 5.5 V; 10 mA ≤ I_{OUT} ≤ 400 mA	–1.0%	±0.5%	+1.0%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation[1]		$V_{O(nom)}$ + 0.5 V ≤ V_{IN} ≤ 5.5 V		0.01		%/V
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation		1 mA ≤ I_{OUT} ≤ 400 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 400 mA		0.0005		
V_{DO}	Dropout voltage[5] (V_{IN} = $V_{OUT(nom)}$ – 0.1 V)		I_{OUT} = 400 mA		75	200	mV
$Z_{O(do)}$	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ V_{OUT} + V_{DO}		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	400	650	800	mA
			3.6 V ≤ V_{IN} ≤ 4.2 V, 0°C ≤ T_J ≤ 70°C	500		800	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		450		mA
I_{REV}	Reverse leakage current[6] ($-I_{IN}$)		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	GND pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 400 mA		800	1000	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5, –40°C ≤ T_J ≤ 100°C		0.02	1	µA
I_{FB}	FB pin current (TPS73601)				0.1	0.3	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 400 mA		58		dB
			f = 10 kHz, I_{OUT} = 400 mA		37		
V_n	Output noise voltage BW = 10Hz – 100KHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
t_{STR}	Startup time		V_{OUT} = 3 V, R_L = 30 Ω C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs
$V_{EN(high)}$	EN pin high (enabled)			1.7		V_{IN}	V
$V_{EN(low)}$	EN pin low (shutdown)			0		0.5	V
$I_{EN(high)}$	EN pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		160		°C
			Reset, temperature decreasing		140		
T_J	Operating junction temperature			–40		125	°C

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) For $V_{OUT(nom)}$ < 1.6 V, when V_{IN} ≤ 1.6 V, the output locks to V_{IN} and may result in a damaging over-voltage level on the output. To avoid this situation, disable the device before powering down the V_{IN}.
(3) TPS73601 is tested at V_{OUT} = 2.5 V.
(4) Tolerance of external resistors not included in this specification.
(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)}$ < 1.8 V.
(6) Fixed-voltage versions only; refer to *Application Information* section for more information.