Quadrature Decoder/Counter Interface ICs

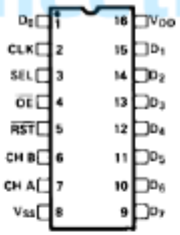
Technical Data

HCTL-2000
HCTL-2016
HCTL-2020

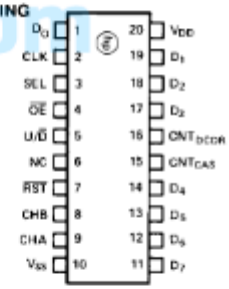
Features

- Interfaces Encoder to Microprocessor
- 14 MHz Clock Operation
- Full 4X Decode
- High Noise Immunity: Schmitt Trigger Inputs Digital Noise Filter
- 12 or 16-Bit Binary Up/ Down Counter
- Latched Outputs
- 8-Bit Tristate Interface
- 8, 12, or 16-Bit Operating Modes
- Quadrature Decoder Output Signals, Up/Down and Count
- Cascade Output Signals, Up/ Down and Count
- Substantially Reduced System Software

DIGITAL MOTION ENCODING



PINOUT A



PINOUT B

Applications

- Interface Quadrature Incremental Encoders to Microprocessors
- Interface Digital Potentiometers to Digital Data Input Buses

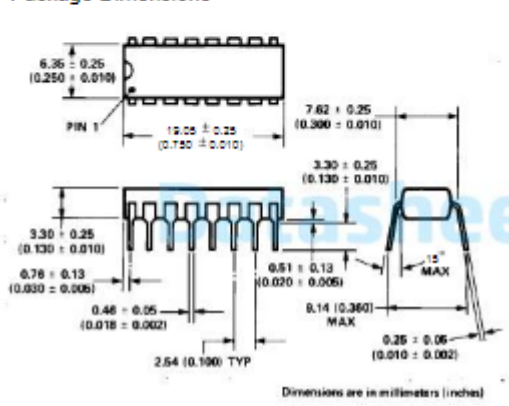
Description

The HCTL-2000, 2016, 2020 are CMOS ICs that perform the quadrature decoder, counter, and bus interface function. The HCTL-20XX family is designed to improve system performance in digital closed loop motion control systems and digital data input systems. It does this by shifting time intensive quadrature decoder functions to a cost effective hardware solution. The entire HCTL-20XX family consists of a 4x quadrature decoder, a binary up/down state counter, and an 8-bit bus interface. The use of Schmitt-triggered CMOS inputs and input noise filters allows reliable operation in noisy environments. The HCTL-2000 contains a 12-bit counter. The HCTL-2016 and 2020 contain a 16-bit counter. The HCTL-2020 also contains quadrature decoder output signals and cascade signals for use with many standard counter ICs. The HCTL-20XX family provides LSTTL compatible tri-state output buffers. Operation is specified for a temperature range from -40 to +85 C° at clock frequencies up to 14 MHz.

Devices

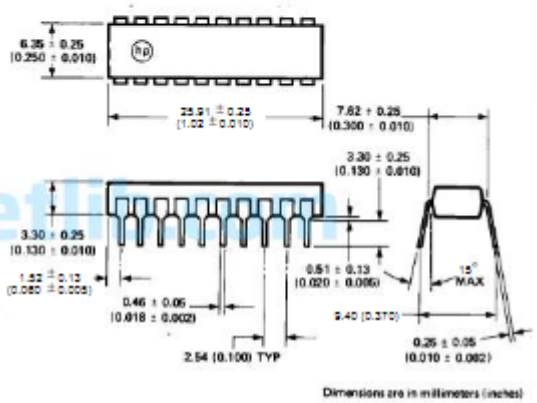
Part Number	Description	Package Drawing
HCTL-2000	12-bit counter. 14 MHz clock operation.	A
HCTL-2016	All features of the HCTL-2000. 16-bit counter.	A
HCTL-2020	All features of the HCTL-2016. Quadrature decoder output signals. Cascade output signals.	B

Package Dimensions



PACKAGE A LEAD FINISH: SOLDER DIPPED

PACKAGE A



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PACKAGE B

Operating Characteristics

Table 1. Absolute Maximum Ratings
(All voltages below are referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	-0.3 to +5.5	V
Input Voltage	V_{IN}	-0.3 to V_{DD} +0.3	V
Storage Temperature	T_S	-40 to +125	°C
Operating Temperature	T_A[1]	-40 to +85	°C

Table 2. Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	+4.5 to +5.5	V
Ambient Temperature	T_A[1]	-40 to +85	°C

Table 3. DC Characteristics V_{DD} = 5 V ± 5%; T_A = -40 to 85 C°

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL} [2]	Low-Level Input Voltage				1.5	V
V_{IH} [2]	High-Level Input Voltage		3.5			V
V_{T+}	Schmitt-Trigger Positive-Going Threshold			3.5	4.0	V
V_{T-}	Schmitt-Trigger Negative-Going Threshold		1.0	1.5		V
V_H	Schmitt-Trigger Hysteresis		1.0	2.0		V
I_{IN}	Input Current	$V_{IN} = V_{SS}$ or V_{DD}	-10	1	+10	µA
V_{OH} [2]	High-Level Output Voltage	I_{OH} -1.6 mA	2.4	4.5		V
V_{OL} [2]	Low-Level Output Voltage	I_{OL} = +4.8 mA		0.2	0.4	V
I_{OZ}	High-Z Output Leakage Current	$V_O = V_{SS}$ or V_{DD}	-10	1	+10	µA
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{SS}$ or V_{DD}, V_O = HiZ		1	5	µA
C_{IN}	Input Capacitance	Any Input [3]		5		pF
C_{OUT}	Output Capacitance	Any Output [3]		6		pF

Notes:
1. Free air.
2. In general, for any V_{DD} between the allowable limits (+4.5 V to +5.5 V), V_{IL} = 0.3 V_{DD} and V_{IH} = 0.7 V_{DD}; typical values are $V_{OH} = V_{DD}$ - 0.5 V @ I_{OH} = -40 µA and $V_{OL} = V_{SS}$ + 0.2 V @ I_{OL} = 1.6 mA.
3. Including package capacitance.

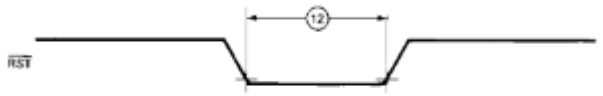
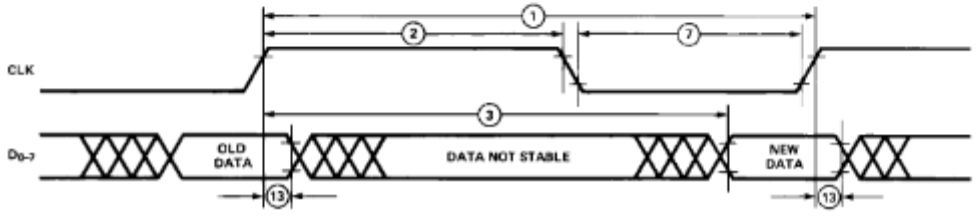


Figure 1. Reset Waveform.



Functional Pin Description

Table 4. Functional Pin Descriptions

Symbol	Pin 2000/2016	Pin 2020	Description
V_{DD}	16	20	Power Supply
V_{SS}	8	10	Ground
CLK	2	2	CLK is a Schmitt-trigger input for the external clock signal.
CHA CHB	7 6	9 8	CHA and CHB are Schmitt-trigger inputs which accept the outputs from a quadrature encoded source, such as incremental optical shaft encoder. Two channels, A and B, nominally 90 degrees out of phase, are required.
$\overline{RST}$	5	7	This active low Schmitt-trigger input clears the internal position counter and the position latch. It also resets the inhibit logic. RST is asynchronous with respect to any other input signals.
$\overline{OE}$	4	4	This CMOS active low input enables the tri-state output buffers. The OE and SEL inputs are sampled by the internal inhibit logic on the falling edge of the clock to control the loading of the internal position data latch.
SEL	3	3	This CMOS input directly controls which data byte from the position latch is enabled into the 8-bit tri-state output buffer. As in OE above, SEL also controls the internal inhibit logic. SEL = 0 → High byte selected; SEL = 1 → Low byte selected
CNT_{DCDR}		16	A pulse is presented on this LSTTL-compatible output when the quadrature decoder has detected a state transition.
$U/\overline{D}$		5	This LSTTL-compatible output allows the user to determine whether the IC is counting up or down and is intended to be used with the CNT_{DCDR} and CNT_{CAS} outputs. The proper signal U (high level) or D (low level) will be present before the rising edge of the CNT_{DCDR} and CNT_{CAS} outputs.
CNT_{CAS}		15	A pulse is presented on this LSTTL-compatible output when the HCTL-2020 internal counter overflows or underflows. The rising edge on this waveform may be used to trigger an external counter.
D0	1	1	These LSTTL-compatible tri-state outputs form an 8-bit output port through which the contents of the 12/16-bit position latch may be read in 2 sequential bytes. The high byte, containing bits 8-15, is read first (on the HCTL-2000, the most significant 4 bits of this byte are set to 0 internally). The lower byte, bits 0-7, is read second.
D1	15	19	
D2	14	18	
D3	13	17	
D4	12	14	
D5	11	13	
D6	10	12	
D7	9	11	
NC		6	Not connected - this pin should be left floating.

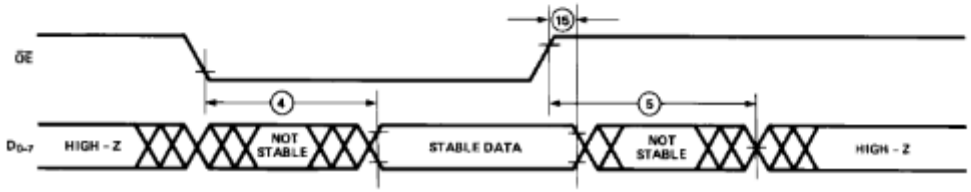
Switching Characteristics

Table 5. Switching Characteristics Min/Max specifications at V$_{DD}$ = 5.0 ± 5%, T$_A$ = -40 to + 85 C.°

	Symbol	Description	Min.	Max.	Units
1	t_{CLK}	Clock period	70		ns
2	t_{CHH}	Pulse width, clock high	28		ns
3	t_{CD} [1]	Delay time, rising edge of clock to valid, updated count information on D0-7		65	ns
4	t_{CDE}	Delay time, $\overline{OE}$ fall to valid data		65	ns
5	t_{CDZ}	Delay time, $\overline{OE}$ rise to Hi-Z state on D0-7		40	ns
6	t_{SDV}	Delay time, SEL valid to stable, selected data byte (delay to High Byte = delay to Low Byte)		65	ns
7	t_{CLH}	Pulse width, clock low	28		ns
8	t_{SS} [2]	Setup time, SEL before clock fall	20		ns
9	t_{OS} [2]	Setup time, $\overline{OE}$ before clock fall	20		ns
10	t_{SH} [2]	Hold time, SEL after clock fall	0		ns
11	t_{OH} [2]	Hold time, $\overline{OE}$ after clock fall	0		ns
12	t_{RST}	Pulse width, RST low	28		ns
13	t_{DCD}	Hold time, last position count stable on D0-7 after clock rise	10		ns
14	t_{DSD}	Hold time, last data byte stable after next SEL state change	5		ns
15	t_{DOD}	Hold time, data byte stable after $\overline{OE}$ rise	5		ns
16	t_{UDD}	Delay time, U/$\overline{D}$ valid after clock rise		45	ns
17	t_{CHD}	Delay time, CNT$_{DCDR}$ or CNT$_{CAS}$ high after clock rise		45	ns
18	t_{CLD}	Delay time, CNT$_{DCDR}$ or CNT$_{CAS}$ low after clock fall		45	ns
19	t_{UDH}	Hold time, U/$\overline{D}$ stable after clock rise	10		ns
20	t_{UDCS}	Setup time, U/$\overline{D}$ valid before CNT$_{DCDR}$ or CNT$_{CAS}$ rise	t_{CLK} -45		ns
21	t_{UDCH}	Hold time, U/$\overline{D}$ stable after CNT$_{DCDR}$ or CNT$_{CAS}$ rise	t_{CLK} -45		ns

Notes:

1. t_{CD} specification and waveform assume latch not inhibited.
2. t_{SS}, t_{OS}, t_{SH}, t_{OH} only pertain to proper operation of the inhibit logic. In other cases, such as 8 bit read operations, these setup and hold times do not need to be observed.



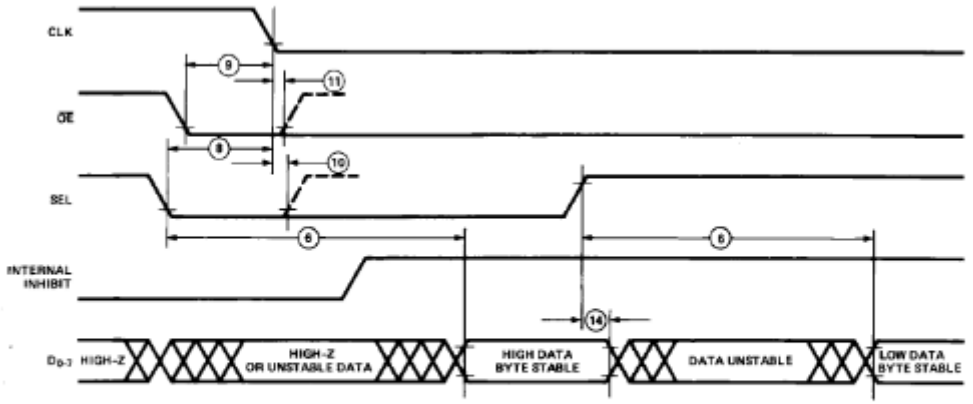


Figure 4. Bus Control Timing.

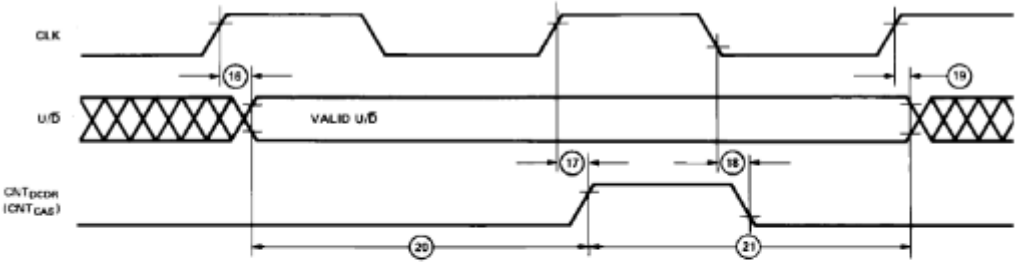


Figure 5. Decoder, Cascade Output Timing (HCTL-2020 only).

Operation

A block diagram of the HCTL-20XX family is shown in Figure 6. The operation of each major function is described in the following sections.

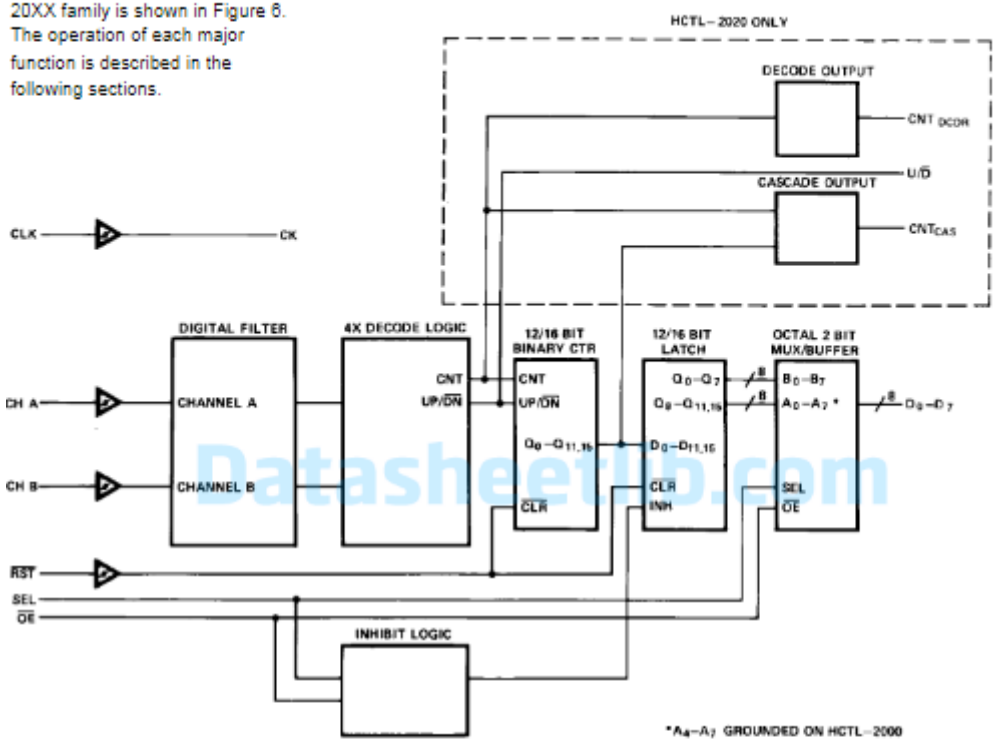


Figure 6. Simplified Logic Diagram.

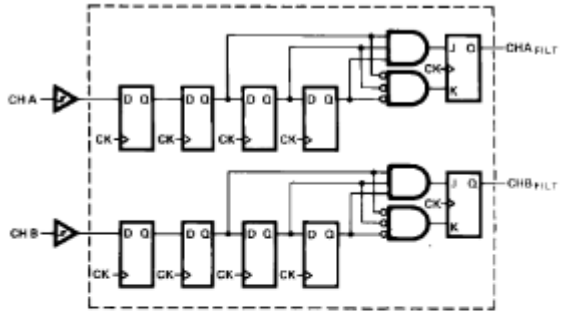


Figure 7. Simplified Digital Noise Filter Logic.

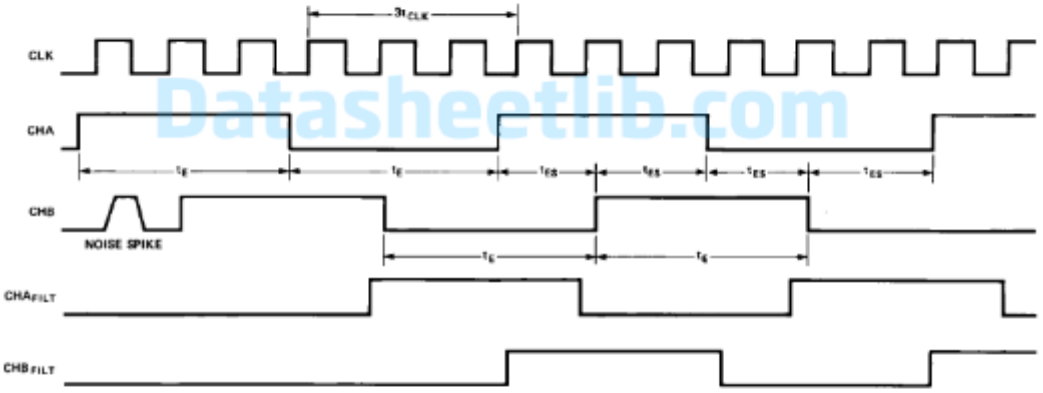


Figure 8. Signal Propagation through Digital Noise Filter.

Digital Noise Filter

The digital noise filter section is responsible for rejecting noise on the incoming quadrature signals. The input section uses two techniques to implement improved noise rejection. Schmitt-trigger inputs and a three-clock-cycle delay filter combine to reject low level noise and large, short duration noise spikes that typically occur in motor system applications. Both common mode and differential mode noise are rejected. The user benefits from these techniques by improved integrity of the data in the counter. False counts triggered by noise are avoided.

Figure 7 shows the simplified schematic of the input section. The signals are first passed through a Schmitt trigger buffer to address the problem of input signals with slow rise times and low level noise (approximately < 1 V). The cleaned up signals are then passed to a four-bit delay filter. The signals on each channel are sampled on rising clock edges. A time history of the signals is stored in the four-bit shift register. Any change on the input is tested for a stable level being present for three consecutive rising clock edges. Therefore, the filtered output waveforms can change only after an input level has the same value for three consecutive rising clock edges. Refer to Figure 8 which shows the timing diagram. The result of this circuitry is that short noise spikes between rising clock edges are ignored and pulses shorter than two clock periods are rejected.

Quadrature Decoder

The quadrature decoder decodes the incoming filtered signals into count information. This circuitry multiplies the resolution of the input signals by a factor of four (4X decoding). When using an encoder for motion sensing, the user benefits from the increased resolution by being able to provide better system control.

The quadrature decoder samples the outputs of the CHA and CHB filters. Based on the past binary state of the two signals and the present state, it outputs a count signal and a direction signal to the internal position counter. In the case of the HCTL-2020, the signals also go to external pins 5 and 16 respectively.

Figure 9 shows the quadrature states and the valid state transitions. Channel A leading channel B results in counting up. Channel B leading channel A results in counting down. Illegal state transitions, caused by faulty encoders or noise severe enough to pass through the filter, will produce an erroneous count.

Design Considerations

The designer should be aware that the operation of the digital filter places a timing constraint on the relationship between incoming quadrature signals and the external clock. Figure 8 shows the timing waveform with an incremental encoder input. Since an input has to be stable for three rising clock edges, the encoder pulse width (t_E - low or high) has to be greater than three clock periods ($3t_{CLK}$). This guarantees that the asynchronous input will be stable during three consecutive rising clock edges. A realistic design also has to take