DATA SHEET

RENESAS

MOS INTEGRATED CIRCUIT

μPD720114

ECOUSB™ Series

USB 2.0 HUB CONTROLLER

The μPD720114 is a USB 2.0 hub device that complies with the Universal Serial Bus (USB) Specification Revision 2.0 and works up to 480 Mbps. USB 2.0 compliant transceivers are integrated for upstream and all downstream ports. The μPD720114 works backward compatible either when any one of the downstream ports is connected to a USB 1.1 compliant device, or when the upstream port is connected to a USB 1.1 compliant host.

Detailed function descriptions are provided in the following user's manual. Be sure to read the manual before designing.

μPD720114 User's Manual: R19UH0079E

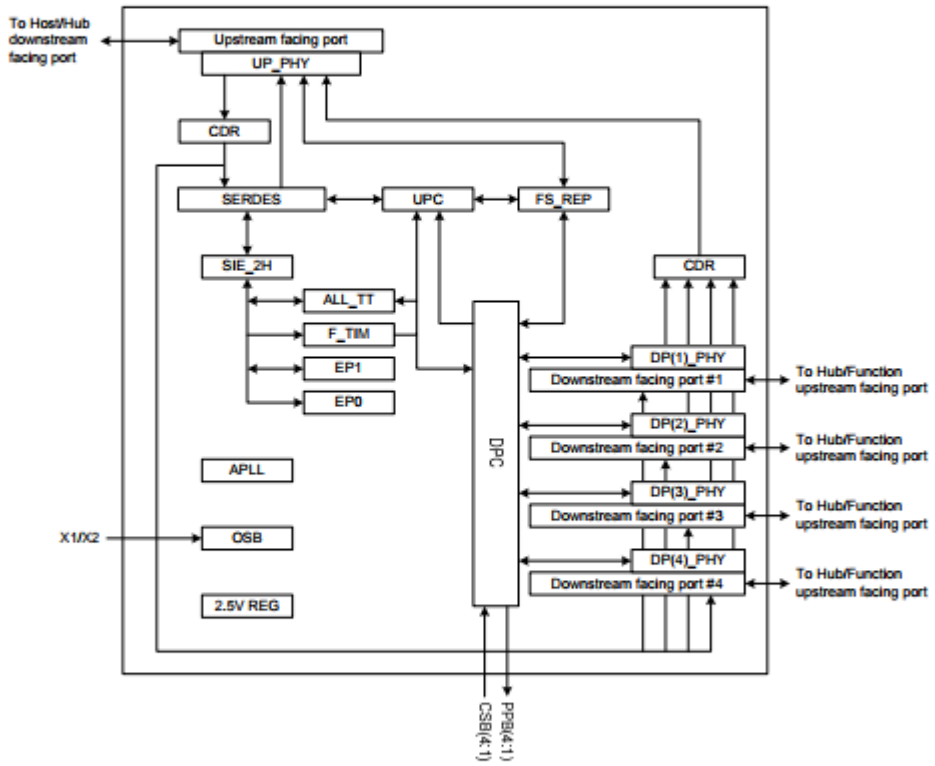
FEATURES

- Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 1.5/12/480 Mbps)
- High-speed or full-speed packet protocol sequencer for Endpoint 0/1
- 4 (Max.) downstream facing ports
- Low power consumption (10 μA when hub in idle status, 149 mA when all parts run in HS mode)
- All downstream facing ports can handle high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction.
- Supports split transaction to handle full-speed and low-speed transaction on downstream facing ports when Hub controller is working in high-speed mode.
- One Transaction Translator per Hub and supports four non-periodic buffers
- Supports self-powered and bus-powered mode
- Supports individual or global over-current detection and individual or ganged power control
- Supports downstream port status with LED
- Supports non-removable devices by I/O pin configuration
- Support Energy Star for PC peripheral system
- On chip Rpu, Rpd resistors and regulator (for core logic)
- Use 30 MHz crystal
- 3.3 V power supply

ORDERING INFORMATION

	Part Number	Package	Remark
	μPD720114GA-9EU-A	48-pin plastic TQFP (Fine pitch) (7 × 7)	Lead-free product
	μPD720114GA-YEU-A	48-pin plastic TQFP (Fine pitch) (7 × 7)	Lead-free product
<R>	μPD720114GA-YEU-AT	48-pin plastic TQFP (Fine pitch) (7 × 7)	Lead-free product
	μPD720114K9-4E4-A	40-pin plastic QFN (6 × 6)	Lead-free product

BLOCK DIAGRAM

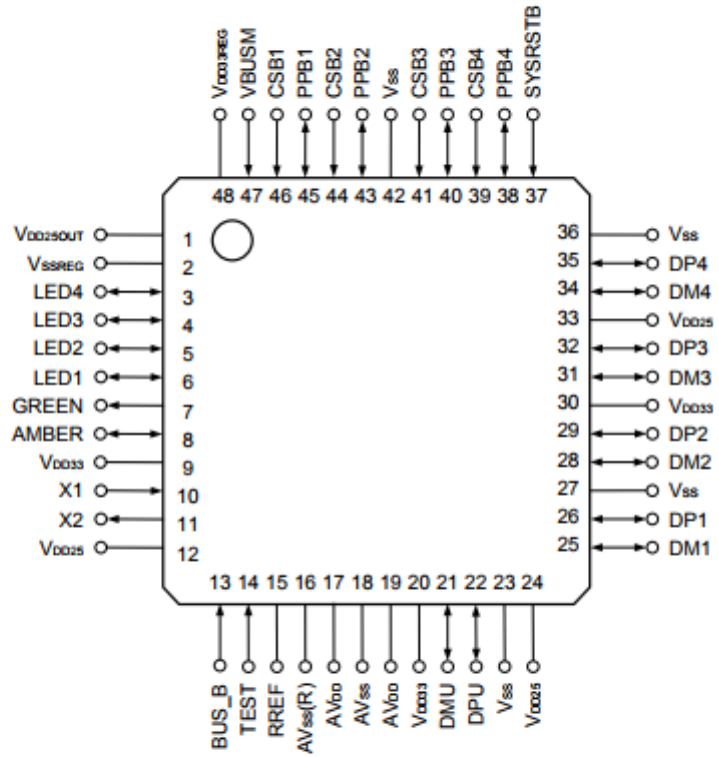


APLL	:	Generates all clocks of Hub.
ALL_TT	:	Translates the high-speed transactions (split transactions) for full/low-speed device to full/low-speed transactions. ALL_TT buffers the data transfer from either upstream or downstream direction. For OUT transaction, ALL_TT buffers data from upstream port and sends it out to the downstream facing ports after speed conversion from high-speed to full/low-speed. For IN transaction, ALL_TT buffers data from downstream ports and sends it out to the upstream facing ports after speed conversion from full/low-speed to high-speed.
CDR	:	Data & clock recovery circuit
DPC	:	Downstream Port Controller handles Port Reset, Enable, Disable, Suspend and Resume
DP(n)_PHY	:	Downstream transceiver supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) transaction
EP0	:	Endpoint 0 controller
EP1	:	Endpoint 1 controller
F_TIM (Frame Timer)	:	Manages hub's synchronization by using micro-SOF which is received at upstream port, and generates SOF packet when full/low-speed device is attached to downstream facing port.
FS_REP	:	Full/low-speed repeater is enabled when the μPD720114 are worked at full-speed mode
OSB	:	Oscillator Block
2.5V REG	:	On chip 2.5V regulator
SERDES	:	Serializer and Deserializer
SIE_2H	:	Serial Interface Engine (SIE) controls USB2.0 and 1.1 protocol sequencer.
UP_PHY	:	Upstream Transceiver supports high-speed (480 Mbps), full-speed (12 Mbps) transaction
UPC	:	Upstream Port Controller handles Suspend and Resume

PIN CONFIGURATION (TOP VIEW)

- **48-pin plastic TQFP (Fine pitch) (7 × 7)**

μPD720114GA-9EU-A
μPD720114GA-YEU-A
<R> μPD720114GA-YEU-AT



Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DDSOUT}	13	BUS_B	25	DM1	37	SYSRSTB
2	V_{SSREG}	14	TEST	26	DP1	38	PPB4
3	LED4	15	RREF	27	V_{SS}	39	CSB4
4	LED3	16	AVss(R)	28	DM2	40	PPB3
5	LED2	17	AV_{DD}	29	DP2	41	CSB3
6	LED1	18	AVss	30	V_{DDIO}	42	V_{SS}
7	GREEN	19	AV_{DD}	31	DM3	43	PPB2
8	AMBER	20	V_{DDIO}	32	DP3	44	CSB2
9	V_{DDIO}	21	DMU	33	V_{DDIS}	45	PPB1
10	X1	22	DPU	34	DM4	46	CSB1
11	X2	23	V_{SS}	35	DP4	47	VBUSM
12	V_{DDIS}	24	V_{DDIS}	36	V_{SS}	48	V_{DDSREG}

Remark AVss(R) should be used to connect RREF through 1 % precision reference resistor of 2.43 kΩ.

1. PIN INFORMATION

Pin Name	I/O	Buffer Type	Active Level	Function
X1	I	2.5 V input		30 MHz Crystal oscillator in
X2	O	2.5 V output		30 MHz Crystal oscillator out
SYSRSTB	I	3.3 V Schmitt input	Low	Asynchronous chip hardware reset
DP(4:1)	I/O	USB D+ signal I/O		USB's downstream facing port D+ signal
DM(4:1)	I/O	USB D− signal I/O		USB's downstream facing port D− signal
DPU	I/O	USB D+ signal I/O		USB's upstream facing port D+ signal
DMU	I/O	USB D− signal I/O		USB's upstream facing port D− signal
BUS_B	I	3.3 V Schmitt input		Power mode select
RREF	A (O)	Analog		Reference resistor connection
CSB1	I	5 V tolerant Schmitt input	Low	Port's over-current status input.
CSB(4:2)	I	3.3 V Schmitt input	Low	Port's over-current status input
PPB(4:1)	I/O	3.3 V output / input	Low	Port's power supply control output or hub configuration input
VBUSM	I	5 V tolerant Schmitt input		Upstream Vaus monitor
AMBER	I/O	3.3V output / input		Amber colored LED control output or port indicator select
GREEN	O	3.3V output		Green colored LED control output or port indicator select
LED(4:1)	I/O	3.3V output / input	Low	LED indicator output show downstream port status or Removable/Non-removable select
TEST	I	3.3 V Schmitt input		Test signal
V_{DDSOUT}				On chip 2.5 V regulator output, it must have a 22 μF (or greater) capacitor to V_{SSREG}
V_{DDIO}				3.3 V V_{DD}
V_{DDSREG}				3.3 V V_{DD} for on chip 2.5 V regulator input, it must have a 4.7 μF (or greater) capacitor to V_{SSREG}
V_{DDIS}				2.5 V V_{DD}. These pins must be supplied from V_{DDSOUT}, output from internal regulator
AV_{DD}				2.5 V V_{DD} for analog circuit
V_{SS}				V_{SS}
V_{SSREG}				On chip 2.5 V regulator V_{SS}
AVss				V_{SS} for analog circuit
AVss(R)				V_{SS} for reference resistor, Connect to AVss.

Remark "5 V tolerant" means that the buffer is 3 V buffer with 5 V tolerant circuit.

2. ELECTRICAL SPECIFICATIONS

2.1 Buffer List

- 2.5 V Oscillator interface
  X1, X2
- 5 V tolerant Schmitt input buffer
  CSB1, VBUSM
- 3.3 V Schmitt input buffer
  CSB(4:2),BUS_B, SYSRSTB, TEST
- 3.3 V I_{OL} = 12 mA output buffer
  GREEN
- 3.3 V input and 3.3 V I_{OL} = 3 mA output buffer
  PPB(4:1), LED(4:1)
- 3.3 V input and I_{OL} = 12 mA output buffer
  AMBER
- USB2.0 interface
  DPU, DMU, DP(4:1), DM(4:1), RREF

Above, "5 V" refers to a 3 V input buffer that is 5 V tolerant (has 5 V maximum input voltage). Therefore, it is possible to have a 5 V connection for an external bus.

2.2 Terminology

Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, $V_{DD33REG}$	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance values for DC current to prevent damage or reduced reliability when current flows out of or into an output pin.
Operating temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

Terms Used in Recommended Operating Range

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, $V_{DD33REG}$	Indicates the voltage range for normal logic operations to occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, applied to the input pins of the device, which indicates the high level state for normal operation of the input buffer. * If a voltage that is equal to or greater than the "Min." value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, applied to the input pins of the device, which indicates the low level state for normal operation of the input buffer. * If a voltage that is equal to or less than the "Max." value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_R	Indicates allowable input rise time to input signal transition time from 0.1 × V_{DD} to 0.9 × V_{DD}.
Input fall time	t_F	Indicates allowable input fall time to input signal transition time from 0.9 × V_{DD} to 0.1 × V_{DD}.

DC Characteristics (V_{DD33} = 3.14 to 3.46 V, T_A = 0 to +70 °C)

Control Pin Block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output leakage current	I_{OZ}	V_O = V_{DD33}, V_{DD3S} or Vss		±10	μA
Output short circuit current	I_{OS} Note			−250	mA
Low-level output current	I_{OL}				
3.3 V low-level output current (3 mA)		V_{OL} = 0.4 V	3		mA
3.3 V low-level output current (12 mA)		V_{OL} = 0.4 V	12		mA
High-level output current	I_{OH}				
3.3 V high-level output current (3 mA)		V_{OH} = 2.4 V	−3		mA
3.3 V high-level output current (12 mA)		V_{OH} = 2.4 V	−12		mA
Input leakage current	I_I				
3.3 V buffer		V_I = V_{DD} or Vss		±10	μA
5.0 V buffer		V_I = V_{DD} or Vss		±10	μA

Note The output short circuit time is measured at one second or less and is tested with only one pin on the LSI.

Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows into a 3-state output pin when it is in a high-impedance state and a voltage is applied to the pin.
Output short circuit current	I_{OS}	Indicates the current that flows from an output pin when it is shorted to GND pins.
Input leakage current	I_I	Indicates the current that flows into an input pin when a voltage is applied to the pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that can flow out of an output pin in the high-level state without reducing the output voltage below the specified V_{OH}. (A negative current indicates current flowing out of the pin.)

2.3 Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD33}, $V_{DD33REG}$		−0.5 to +4.6	V
Input/output voltage	V_I/V_O			
3.3 V input/output voltage		3.0 V ≤ V_{DD33} ≤ 3.6 V V_I /V_O < V_{DD33} + 1.0 V	−0.5 to +4.6	V
5 V input/out voltage		3.0 V ≤ V_{DD33} ≤ 3.6 V V_I /V_O < V_{DD33} + 3.0 V	−0.5 to +6.6	V
Output current	I_O	I_{OL} = 3 mA I_{OL} = 12 mA	10 40	mA mA
Operating temperature	T_A		0 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

Recommended Operating Ranges

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD33}, $V_{DD33REG}$	3.3 V for V_{DD33} pins	3.14	3.30	3.46	V
High-level input voltage	V_{IH}					
3.3 V High-level input voltage			2.0		V_{DD33}	V
5.0 V High-level input voltage			2.0		5.5	V
Low-level input voltage	V_{IL}					
3.3 V Low-level input voltage			0		0.8	V
5.0 V Low-level input voltage			0		0.8	V
Hysteresis voltage	V_H					
5 V Hysteresis voltage			0.3		1.5	V
3.3 V Hysteresis voltage			0.2		1.0	V
Input rise time for SYSRSTB	t_{ist}				10	ms
Input rise time	t_{ir}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{if}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

USB Interface Block

Parameter	Symbol	Conditions	Min.	Max.	Unit
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Termination voltage for upstream facing port pullup (full-speed)	V_{TERM}		3.0	3.6	V
Input Levels for Low-/full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	V
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	|(D+) − (D−)|	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Low-/full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to GND	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		−50	+500	mV
High-speed differential input signaling levels	See Figure 2-4.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		−10.0	+10	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		−10.0	+10	mV
Chirp J level (different signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V_{CHIRPK}		−900	−500	mV