24AA16/24LC16B

16K I²C™ Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Max Clock Frequency	Temp Ranges
24AA16	1.8-5.5	400 kHz(1)	I
24LC16B	2.5-5.5	400 kHz	I, E

Note 1: 100 kHz for Vcc <2.5V

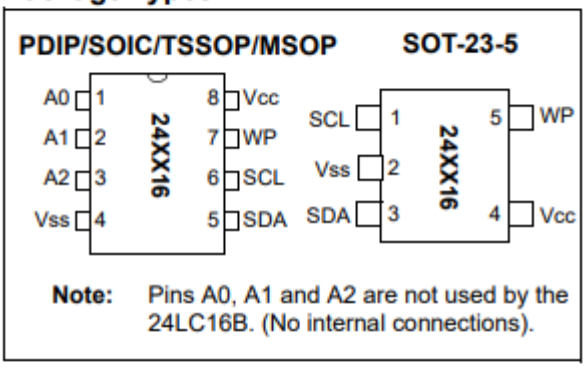
Features

- Single supply with operation down to 1.8V
- Low-power CMOS technology
  - 1 mA active current typical
  - 1 µA standby current (max.) (I-temp)
- Organized as 8 blocks of 256 bytes (8 x 256 x 8)
- 2-wire serial interface bus, I²C™ compatible
- Schmitt Trigger inputs for noise suppression
- Output slope control to eliminate ground bounce
- 100 kHz (2.5V) and 400 kHz (≥2.5V) compatibility
- Self-timed write cycle (including auto-erase)
- Page write buffer for up to 16 bytes
- 2 ms typical write cycle time for page write
- Hardware write-protect for entire memory
- Can be operated as a serial ROM
- Factory programming (QTP) available
- ESD protection > 4,000V
- 1,000,000 erase/write cycles
- Data retention > 200 years
- 8-lead PDIP, SOIC, TSSOP and MSOP packages
- 5-lead SOT-23 package
- Standard and Pb-free finishes available
- Available temperature ranges:
  - Industrial (I): -40°C to +85°C
  - Automotive (E): -40°C to +125°C

Description

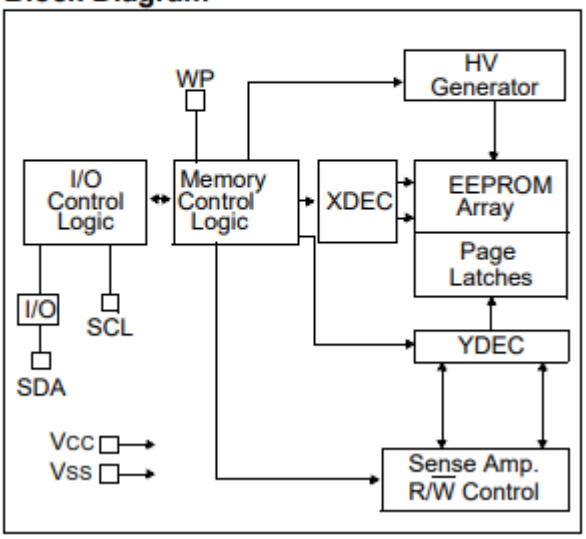
The Microchip Technology Inc. 24AA16/24LC16B (24XX16*) is a 16 Kbit Electrically Erasable PROM. The device is organized as eight blocks of 256 x 8-bit memory with a 2-wire serial interface. Low-voltage design permits operation down to 1.8V with standby and active currents of only 1 µA and 1 mA, respectively. The 24XX16 also has a page write capability for up to 16 bytes of data. The 24XX16 is available in the standard 8-pin PDIP, surface mount SOIC, TSSOP and MSOP packages and is also available in the 5-lead SOT-23 package.

Package Types



Note: Pins A0, A1 and A2 are not used by the 24LC16B. (No internal connections).

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS ..... -0.3V to VCC +1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-65°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			VCC = +1.8V to +5.5V Industrial (I): TA = -40°C to +85°C Automotive (E): TA = -40°C to +125°C				
Param. No.	**Symbol**	**Characteristic**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
D1	VIH	**WP, SCL and SDA pins**	—	—	—	—	—
D2	—	High-level input voltage	0.7 VCC	—	—	V	—
D3	VIL	Low-level input voltage	—	—	0.3 VCC	V	—
D4	VHYS	Hysteresis of Schmitt Trigger inputs	.05 VCC	—	—	V	**(Note 1)**
D5	VOL	Low-level output voltage	—	—	0.40	V	IOL = 3.0 mA, VCC = 2.5V
D6	ILI	**Input leakage current**	—	—	±1	µA	VIN =.1V to VCC
D7	ILO	**Output leakage current**	—	—	±1	µA	VOUT =.1V to VCC
D8	CIN, COUT	Pin capacitance (all inputs/outputs)	—	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D9	ICC write	**Operating current**	—	—	3	mA	VCC = 5.5V, SCL = 400 kHz
D10	ICC read		—	0.01	1	mA	—
D11	ICCS	**Standby current**	— —	0.3 .01	1 5	µA µA	Industrial Automotive SDA = SCL = VCC WP = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

2: Typical measurements taken at room temperature.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			V_{CC} = +1.8V to +5.5V Industrial (I): T_A = -40°C to +85°C Automotive (E): T_A = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Min**	**Max**	**Units**	**Conditions**
1	F_{CLK}	Clock frequency	— —	400 100	kHz	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
2	T_{HIGH}	Clock high time	600 4000	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
3	T_{LOW}	Clock low time	1300 4700	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
4	T_R	SDA and SCL rise time **(Note 1)**	— —	300 1000	ns	2.5V ≤ V_{CC} ≤ 5.5V **(Note 1)** 1.8V ≤ V_{CC} < 2.5V **(24AA16)** **(Note 1)**
5	T_F	SDA and SCL fall time	—	300	ns	**(Note 1)**
6	$T_{HD:STA}$	Start condition hold time	600 4000	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
7	$T_{SU:STA}$	Start condition setup time	600 4700	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
8	$T_{HD:DAT}$	Data input hold time	0	—	ns	**(Note 2)**
9	$T_{SU:DAT}$	Data input setup time	100 250	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
10	$T_{SU:STO}$	Stop condition setup time	600 4000	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
11	T_{AA}	Output valid from clock **(Note 2)**	— —	900 3500	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
12	T_{BUF}	Bus free time: Time the bus must be free before a new transmission can start	1300 4700	— —	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} < 2.5V **(24AA16)**
13	T_{OF}	Output fall time from V_{IH} minimum to V_{IL} maximum	20+0.1C_B —	250 250	ns	2.5V ≤ V_{CC} ≤ 5.5V 1.8V ≤ V_{CC} <2.5V **(24AA16)**
14	T_{SP}	Input filter spike suppression (SDA and SCL pins)	—	50	ns	**(Notes 1 and 3)**
15	T_{WC}	Write cycle time (byte or page)	—	5	ms	—
16	—	Endurance	1M	—	cycles	25°C, **(Note 4)**

Note 1: Not 100% tested. C_B = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined T_{SP} and V_{HYS} specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a T_I specification for standard operation.

4: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site: www.microchip.com.

FIGURE 1-1: BUS TIMING DATA

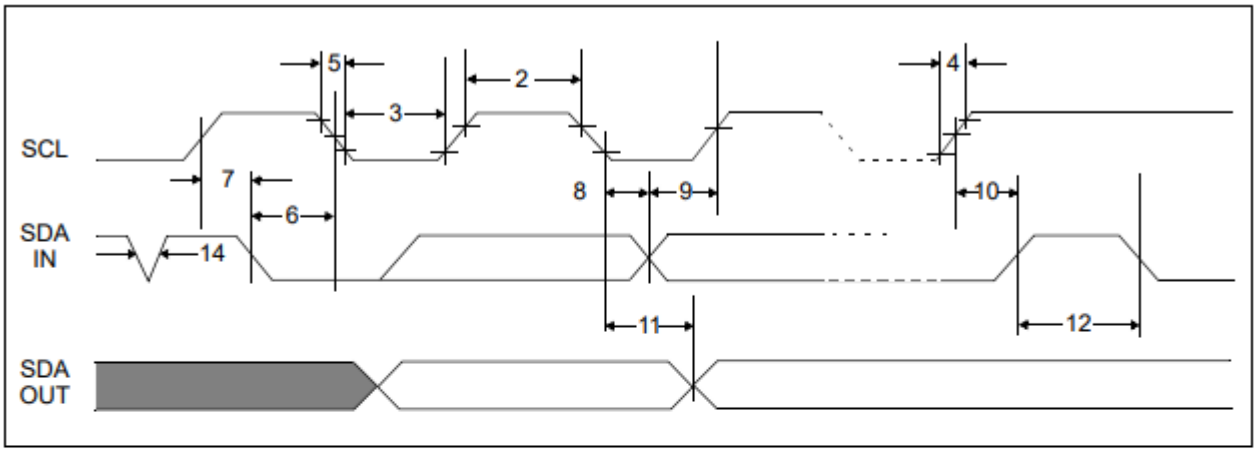
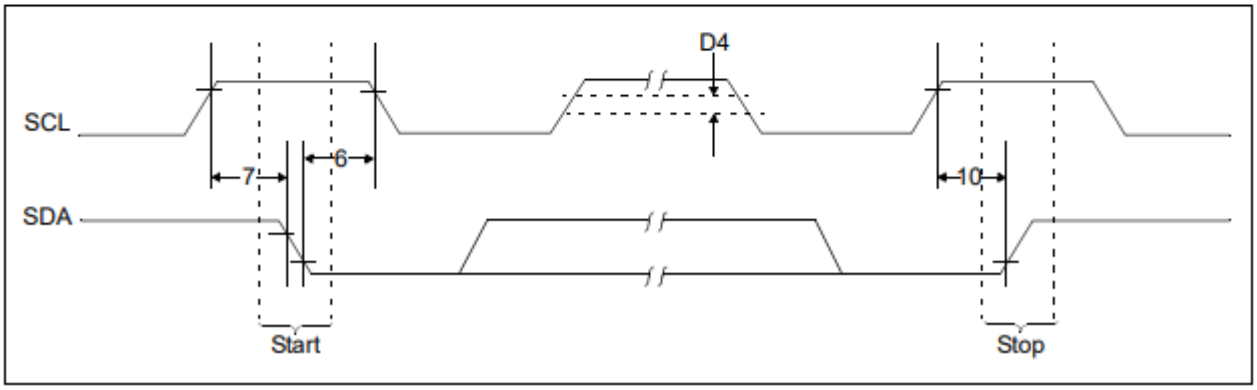


FIGURE 1-2: BUS TIMING START/STOP



2.0 FUNCTIONAL DESCRIPTION

The 24XX16 supports a bidirectional, 2-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter, while a device receiving data is defined as a receiver. The bus has to be controlled by a master device which generates the serial clock (SCL), controls the bus access and generates the Start and Stop conditions, while the 24XX16 works as slave. Both master and slave can operate as transmitter or receiver, but the master device determines which mode is activated.

3.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 3-1).

3.1 Bus not Busy (A)

Both data and clock lines remain high.

3.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

3.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must be ended with a Stop condition.

3.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of data bytes transferred between Start and Stop conditions is determined by the master device and is, theoretically unlimited, (although only the last sixteen will be stored when doing a write operation). When an overwrite does occur it will replace data in a first-in first-out (FIFO) fashion.

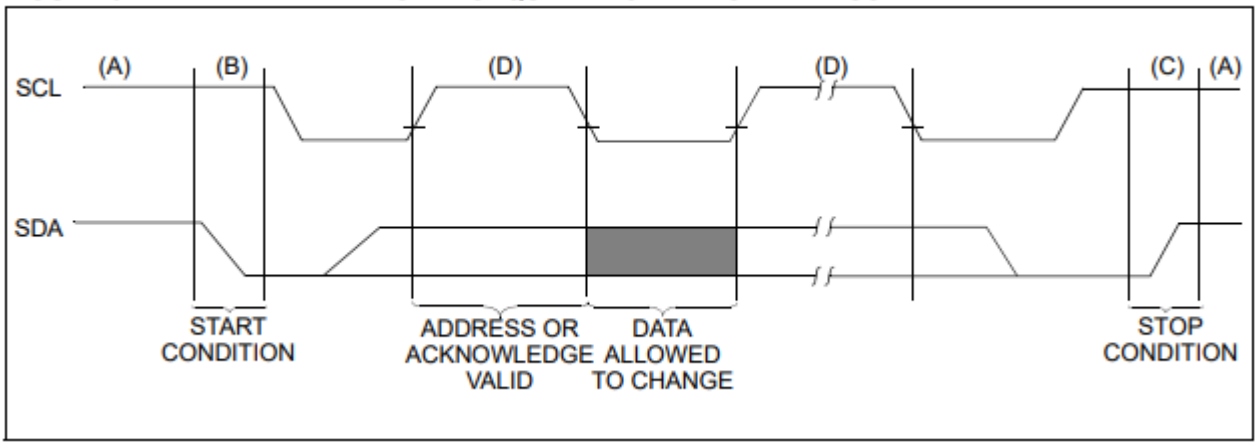
3.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX16 does not generate any Acknowledge bits if an internal programming cycle is in progress.

The device that acknowledges, has to pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge related clock pulse. Of course, setup and hold times must be taken into account. During reads, a master must signal an end of data to the slave by not generating an Acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave (24XX16) will leave the data line high to enable the master to generate the Stop condition.

FIGURE 3-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS



3.6 Device Addressing

A control byte is the first byte received following the Start condition from the master device (Figure 3-2). The control byte consists of a four-bit control code. For the 24XX16, this is set as '1010' binary for read and write operations. The next three bits of the control byte are the block-select bits (B2, B1, B0). They are used by the master device to select which of the eight 256 word-blocks of memory are to be accessed. These bits are in effect the three Most Significant bits of the word address. It should be noted that the protocol limits the size of the memory to eight blocks of 256 words, therefore the protocol can support only one 24XX16 per system.

The last bit of the control byte defines the operation to be performed. When set to '1', a read operation is selected. When set to '0', a write operation is selected. Following the Start condition, the 24XX16 monitors the SDA bus checking the device type identifier being transmitted and, upon receiving a '1010' code, the slave device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the 24XX16 will select a read or write operation.

Operation	Control Code	Block Select	R/$\overline{W}$
Read	1010	Block Address	1
Write	1010	Block Address	0

FIGURE 3-2: CONTROL BYTE ALLOCATION